



User Guide

EVB-ATEK250P3-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	10.07.2021	Initial Version	
1.1	24.09.2021	Component Updated	3/5

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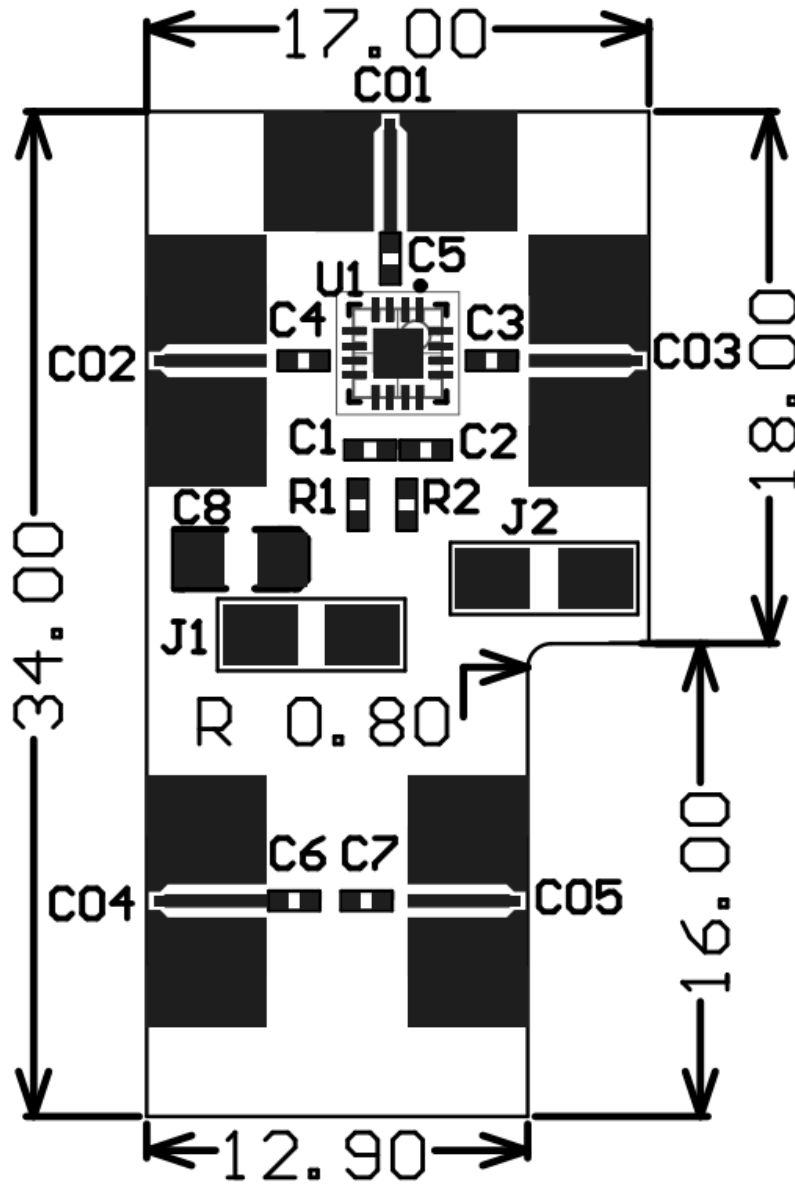
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1 GENERAL INFORMATION



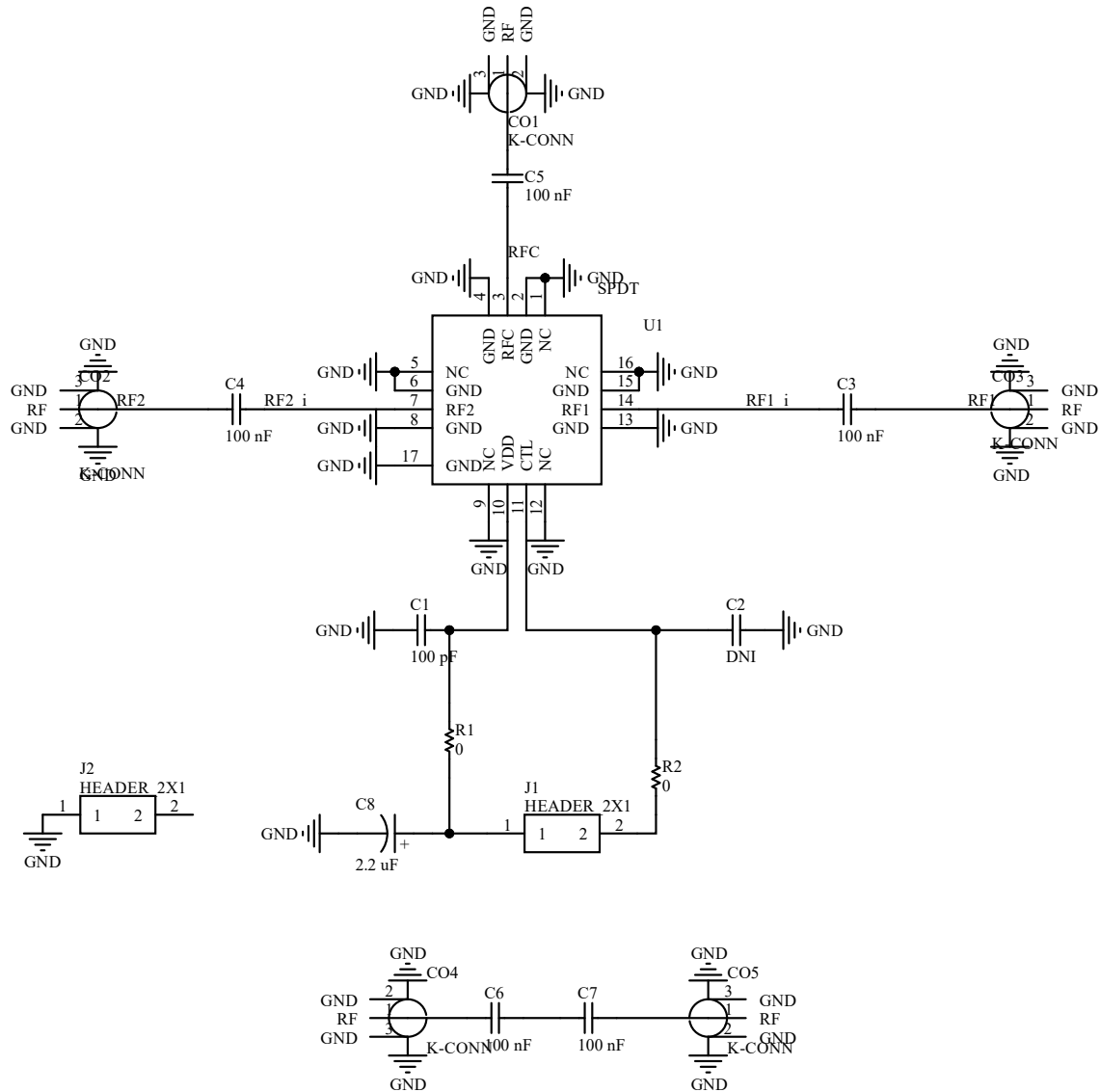
PIN Name	Definition	Comment
C01	RF IN	SMA Connector
C02, C03	RF OUT	SMA Connector
C04, C05	RF Thru Line IO	SMA Connector
J1 Right	CTRL	2.54mm Header
J1 Left	VDD	2.54mm Header
J2 Right	GND	2.54mm Header
J2 Left	N/A	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



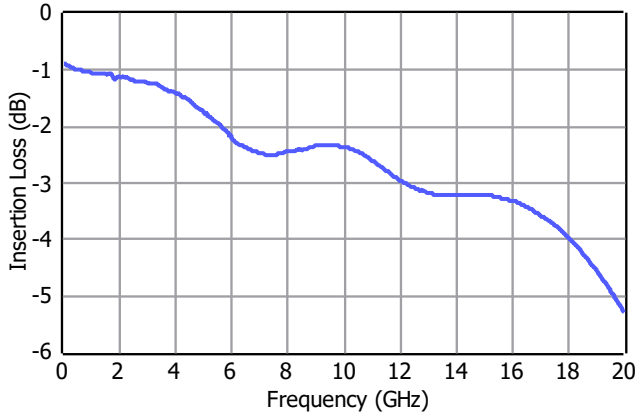
2.2 BOM

Designator	Footprint	Qty	Comment	PN
CO1, CO2, CO3, CO4, CO5	K Connector	5	SMA Connector	
J1, J2	2x1 Header	2	2x1 Header	
C3, C4, C5, C6, C7	0402	5	100 nF	
C8	CASEA	1	2.2 uF	
C1	0402	1	100 pF	
C2	0402	1	DNP	
R1, R2	0402	2	OR	
U1	ATEKQ3316	1	SPDT	ATEK250 P51

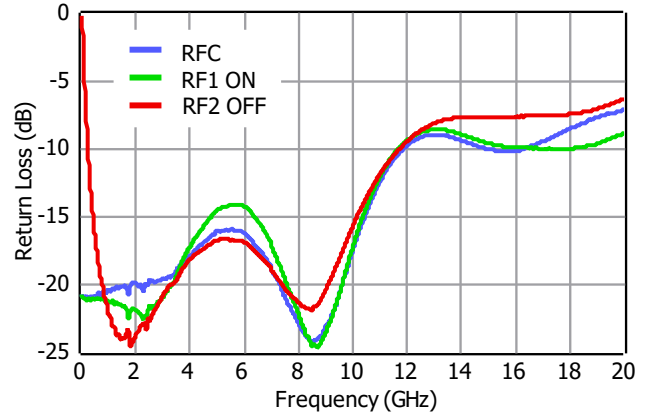
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: $V_{CTRL} = 5\text{ V}$, $T = 25\text{ C}$, CW. For details, please refer to the datasheet.

Insertion Loss



Return Loss



Isolation from RFC to RF2

