User Guide
EVB-ATEK251P4-01

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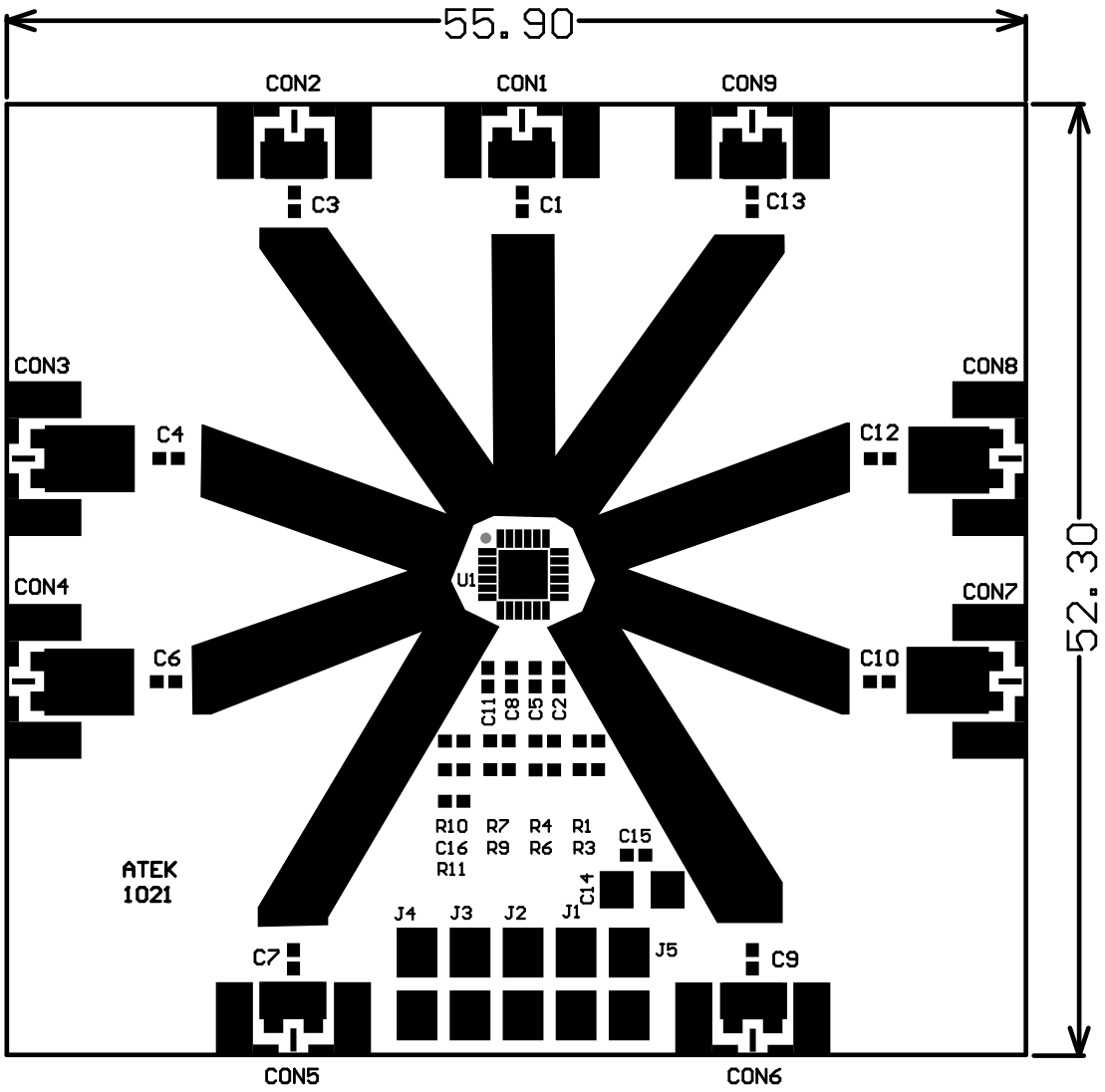
Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	07.07.2021	Initial Version	
1.1	17.09.2021	Conditions Edited	5/5

INDEX

1 GENERAL INFORMATION 3
2 DESIGN INFORMATION 4
2.1 SCHEMATIC 4
2.2 BOM 4
3 TYPICAL PERFORMANCE PLOTS 5

1 GENERAL INFORMATION



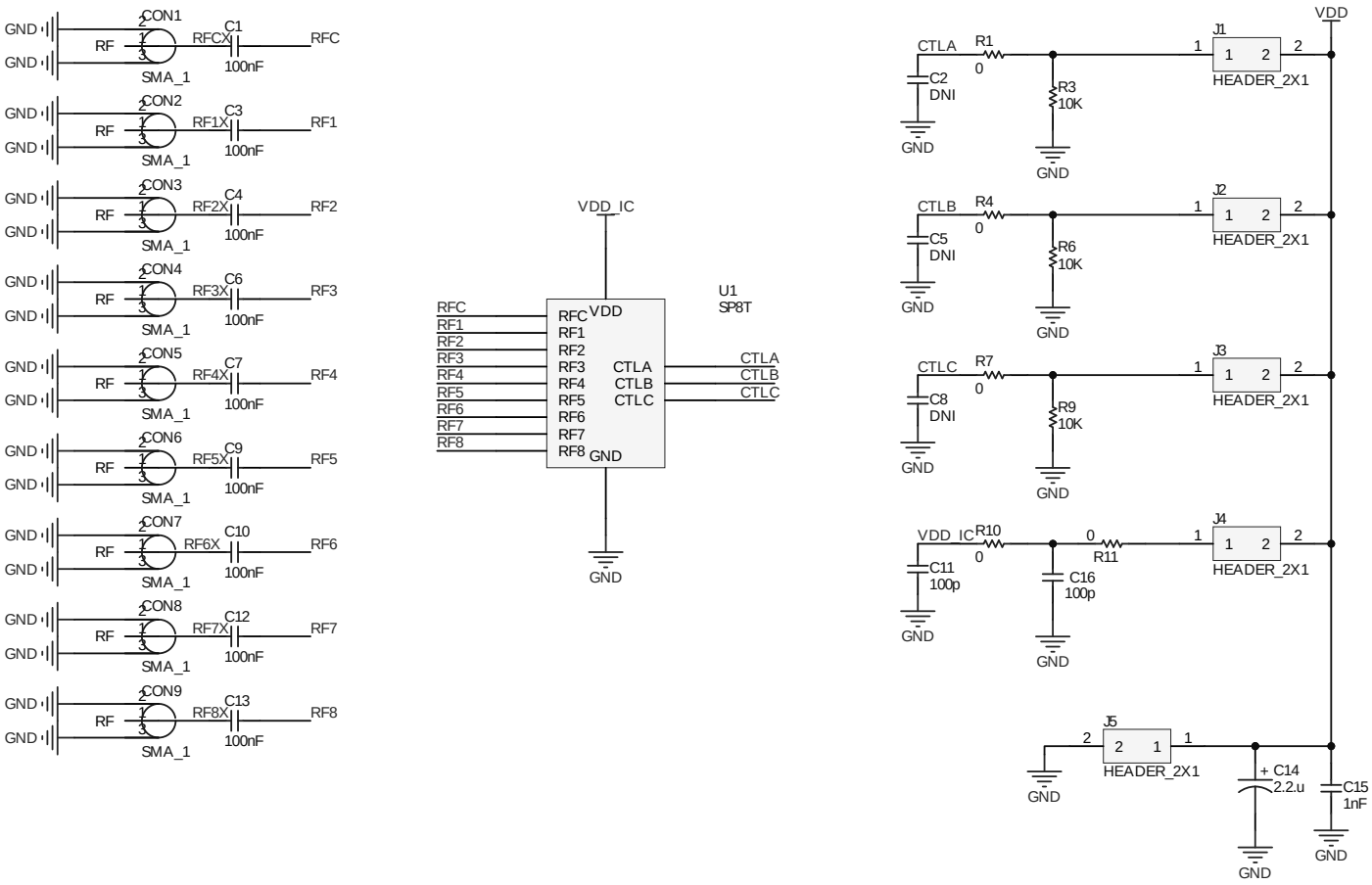
PIN Name	Definition	Comment
CO1	RF IN	SMA Connector
CO2, CO3, CO4, CO5, CO6, CO7, CO8, CO9	RF OUT	SMA Connector
J1 Up, J1 Down, J2 Up, J3 Up, J4 Up, J5 Up	VDD	2.54mm Header
J5 Down	GND	2.54mm Header
J4 Down	CTRL A	2.54mm Header
J3 Down	CTRL B	2.54mm Header
J2 Down	CTRL C	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



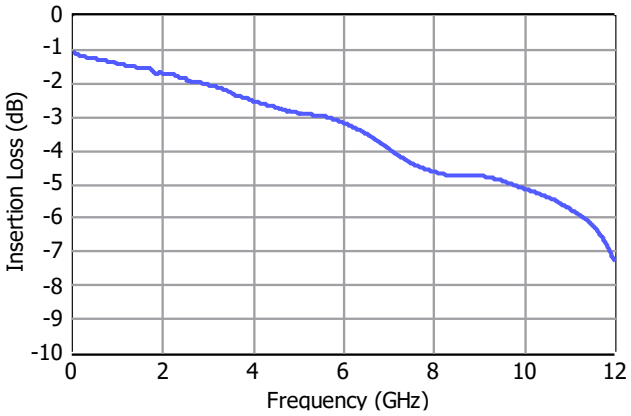
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C3, C4, C6, C7, C9, C10, C12, C13	0402	9	100nF	
C2, C5, C8	0402	3	DNP	
C11, C16	0402	1	0.1uF	
C14	CASEA	1	2.2uF	
C15	0402	1	1nF	
CON1, CON2, CON3, CON4, CON5, CON6, CON7, CON8, CON9	SMA Connector	9	SMA Connector	
J1, J2, J3, J4, J5	HEADER_2X1_V2	5	HEADER_2X1	
R1, R4, R7, R10, R11	0402	5	0R	
R3, R6, R9	0402	3	10K	
U1	ATEKQ4424	1	SP8T	ATEK251 P51

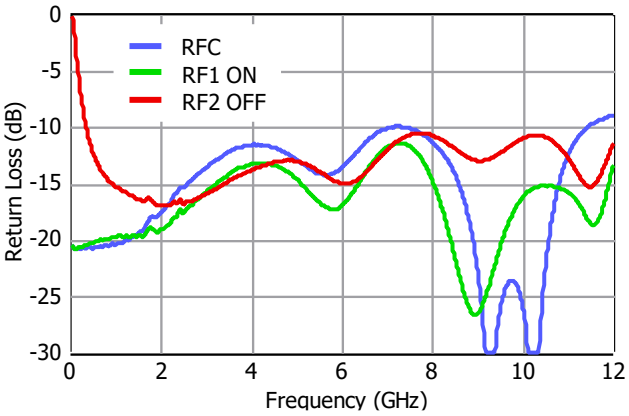
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: V_{CTRL} =0 V / 5 V, T = 25 C, CW. For details, please refer to the datasheet.

Insertion Loss



Return Loss



Isolation from RFC to RF2