

User Guide

EVB-ATEK351P4-01

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	29.07.2021	Initial Version	

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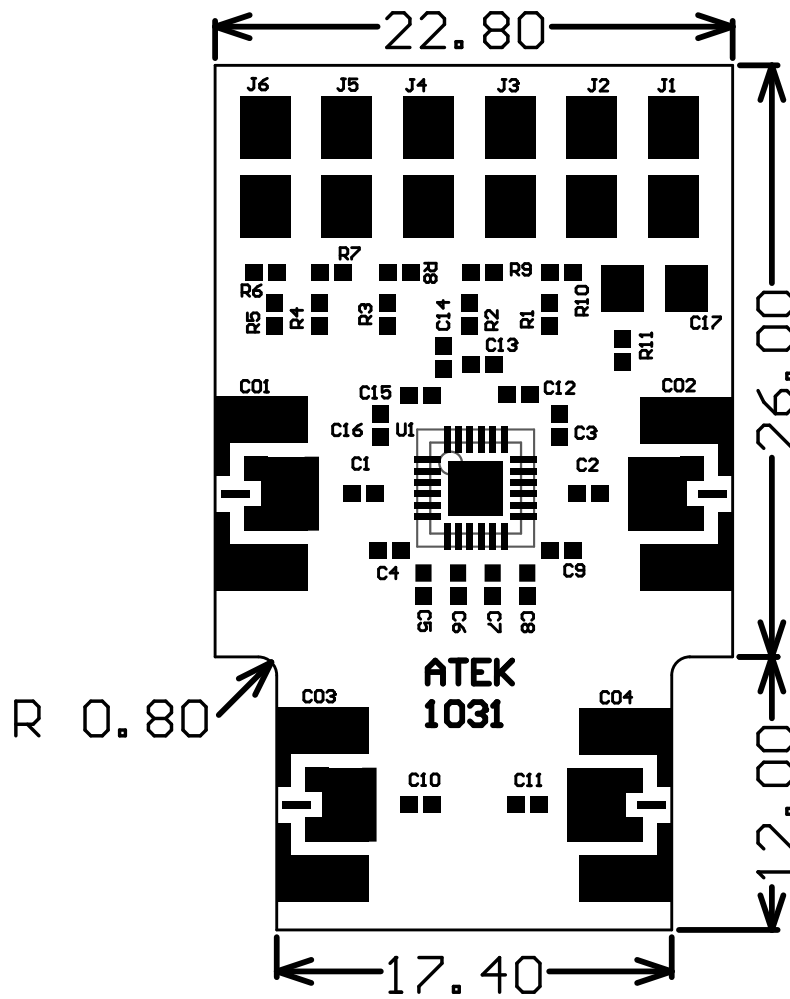
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1 GENERAL INFORMATION



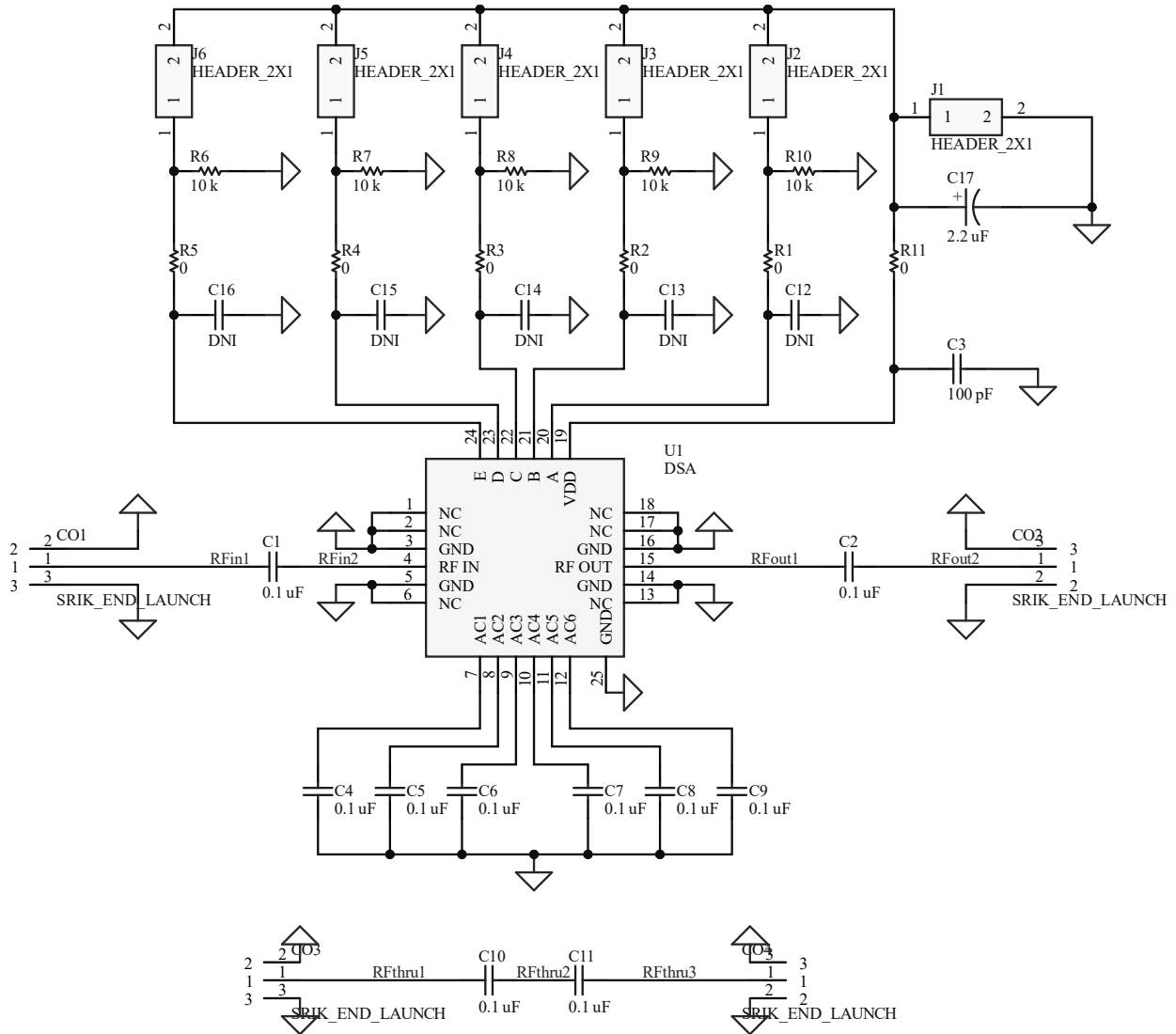
PIN Name	Definition	Comment
CO1	RF IN	SMA Connector
CO2	RF OUT	SMA Connector
CO3, CO4	RF Thru Line IO	SMA Connector
J1 Up	VDD	2.54mm Header
J1 Down	GND	2.54mm Header
J2 Up	P1 – CTRLA	2.54mm Header
J3 Up	P2 – CTRLB	2.54mm Header
J4 Up	P3 – CTRLC	2.54mm Header
J5 Up	P4 – CTRLD	2.54mm Header
J6 Up	P5 – CTRL E	2.54mm Header
J2 Down, J3 Down, J4 Down, J5 Down, J6 Down	N/A	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



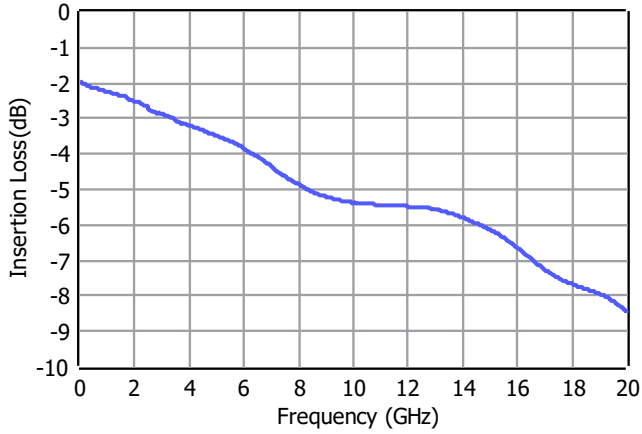
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C01, C02, C03, C04	SMA Connector	4	SMA Connector	
J1, J2, J3, J4, J5, J6	HEADER_2X1	6	HEADER_2X1	
R1, R2, R3, R4, R5, R11	0402	6	0R	
R6, R7, R8, R9, R10	0402	5	10K	
C17	CASEA	1	2.2 uF	
C1, C2, C4, C5, C6, C7, C8, C9, C10, C11	0402	10	0.1 uF	
C3	0402	1	100 pF	
C12, C13, C14, C15, C16	0402	5	DNP	
U1	ATEKQ4424	1	DSA 5 Bit	ATEK351 P50

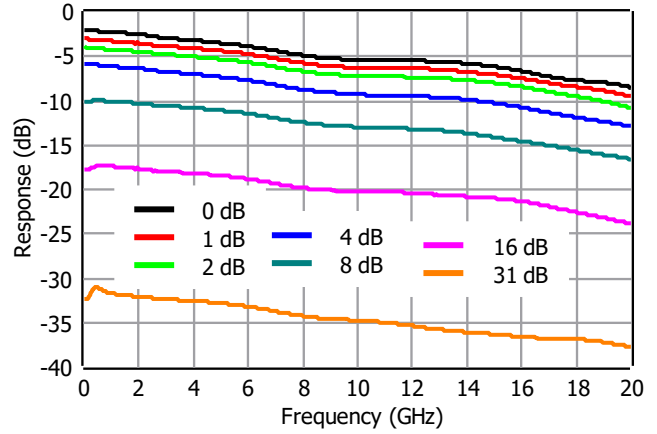
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: Typical, $V_{DD} = 5\text{ V}$, $T = 25\text{ C}$, CW. For details, please refer to the datasheet.

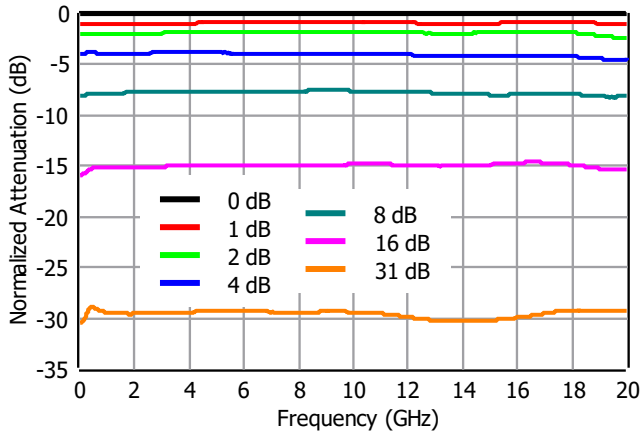
Insertion Loss



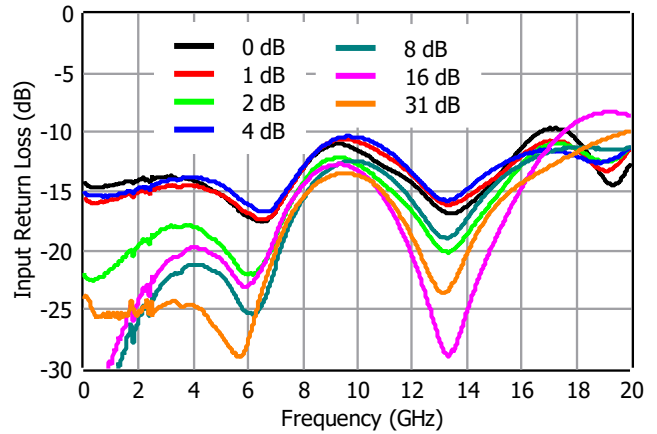
Insertion Loss vs. Attenuation State



Normalized Attenuation



Input Return Loss



Output Return Loss

