

# User Guide

## EVB-ATEK356P3-01

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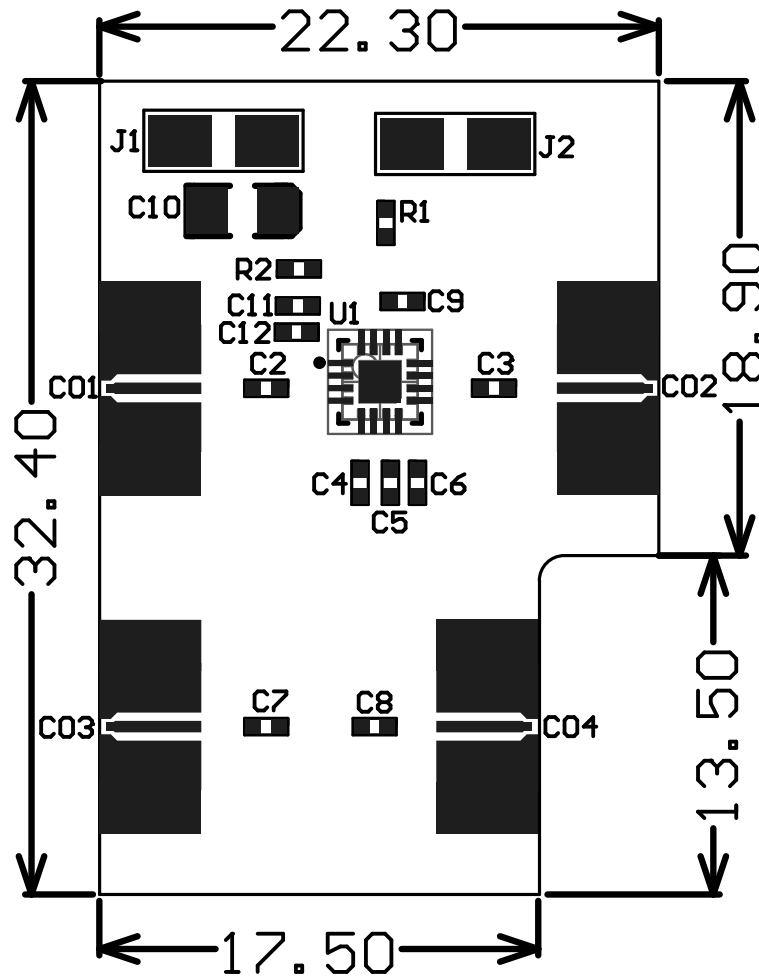
**Revisions**

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	29.07.2021	Initial Version	

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1 GENERAL INFORMATION



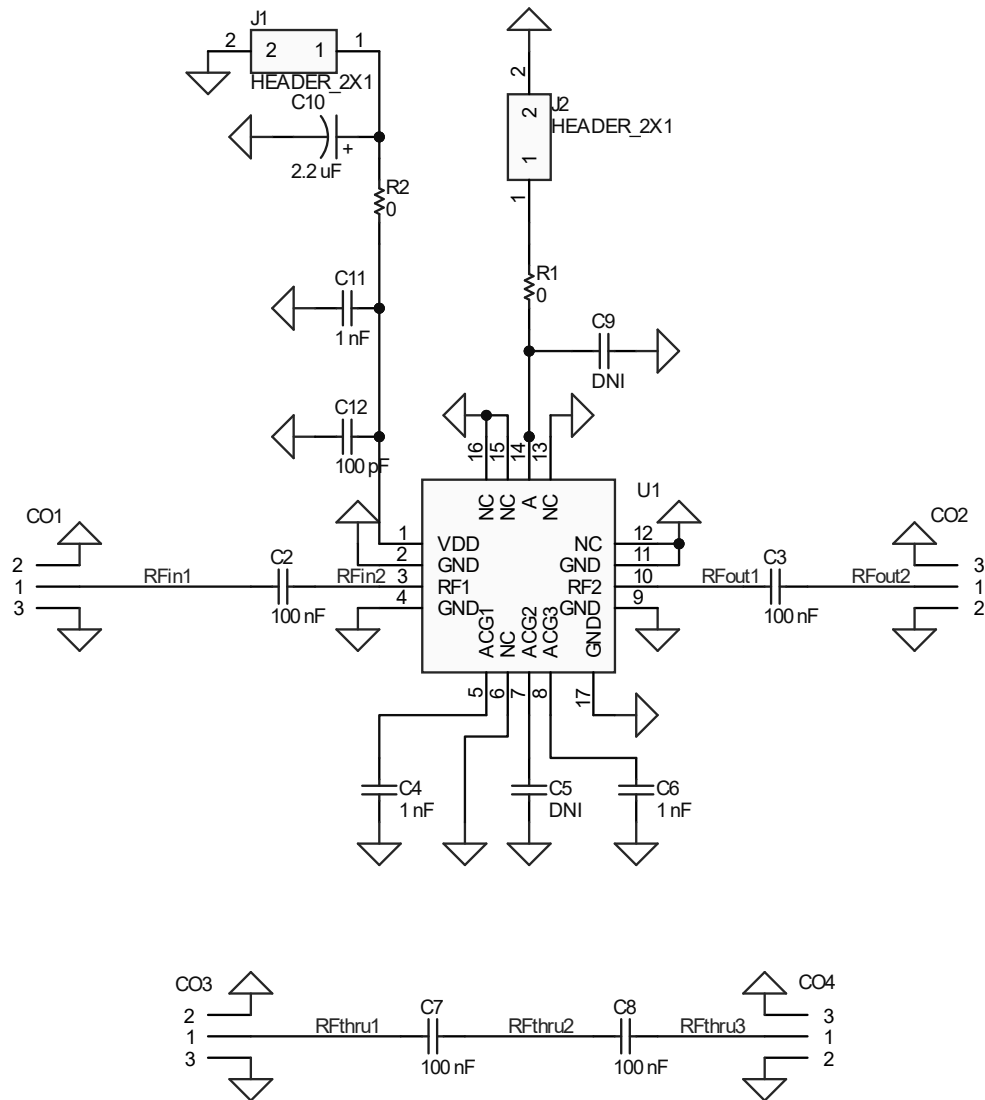
PIN Name	Definition	Comment
<b>CO1</b>	RF IN	SMA Connector
<b>CO2</b>	RF OUT	SMA Connector
<b>CO3, CO4</b>	RF Thru Line IO	SMA Connector
<b>J1 Right</b>	VDD	2.54mm Header
<b>J1 Left, J2 Right</b>	GND	2.54mm Header
<b>J2 Left</b>	P1 – CTRLA	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



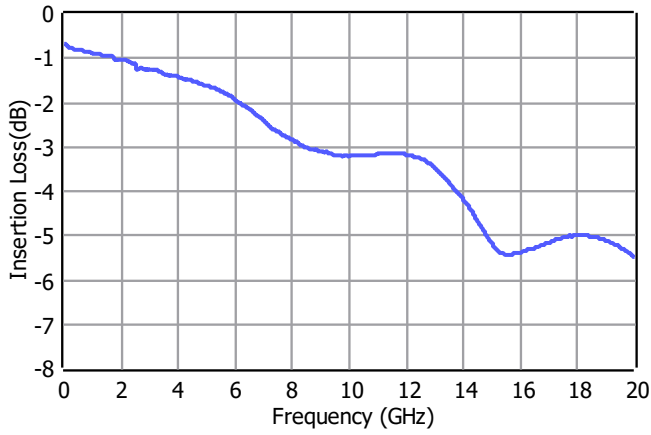
2.2 BOM

Designator	Footprint	Qty	Comment	PN
<b>CO1, CO2, CO3, CO4</b>	SMA Connector	4	SMA Connector	
<b>J1, J2</b>	HEADER_2X1	2	HEADER_2X1	
<b>R1, R2</b>	0402	2	OR	
<b>C2, C3, C7, C8</b>	0402	4	100 nF	
<b>C5, C9</b>	0402	2	DNP	
<b>C10</b>	CASEA	1	2.2 uF	
<b>C4, C6, C11</b>	0402	3	1 nF	
<b>C12</b>	0402	1	100 pF	
<b>U1</b>	ATEKQ3316	1	DSA 1 Bit	ATEK356 P51

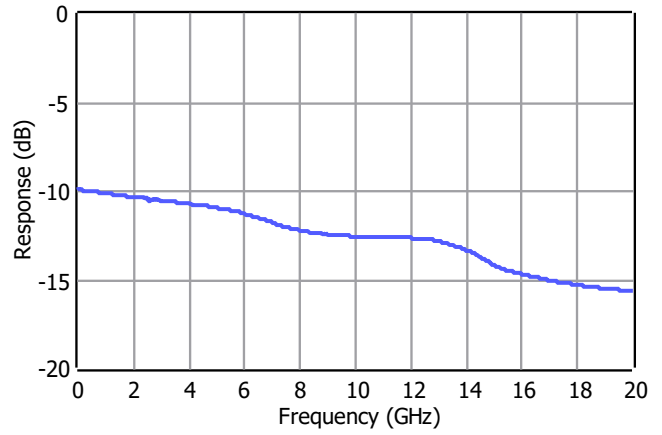
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: Typical,  $V_{DD} = 5\text{ V}$ ,  $T = 25\text{ C}$ , CW. For details, please refer to the datasheet.

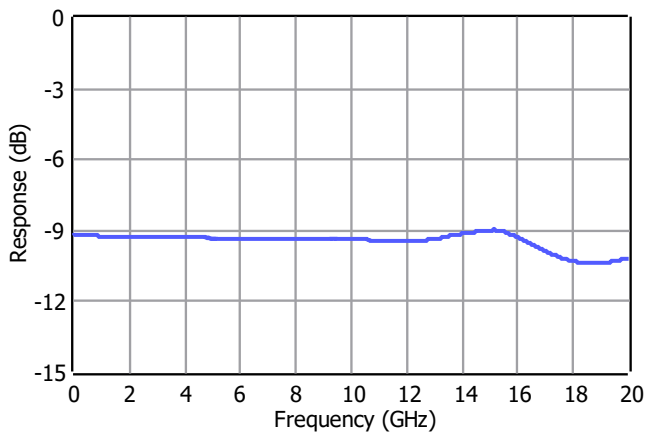
Insertion Loss



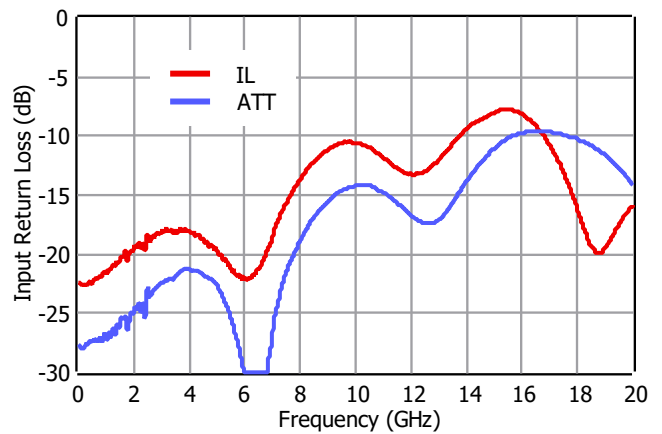
Insertion Loss vs. Attenuation State



Relative Attenuation



Input Return Loss



Output Return Loss

