



User Guide

EVB-ATEK357P4-01

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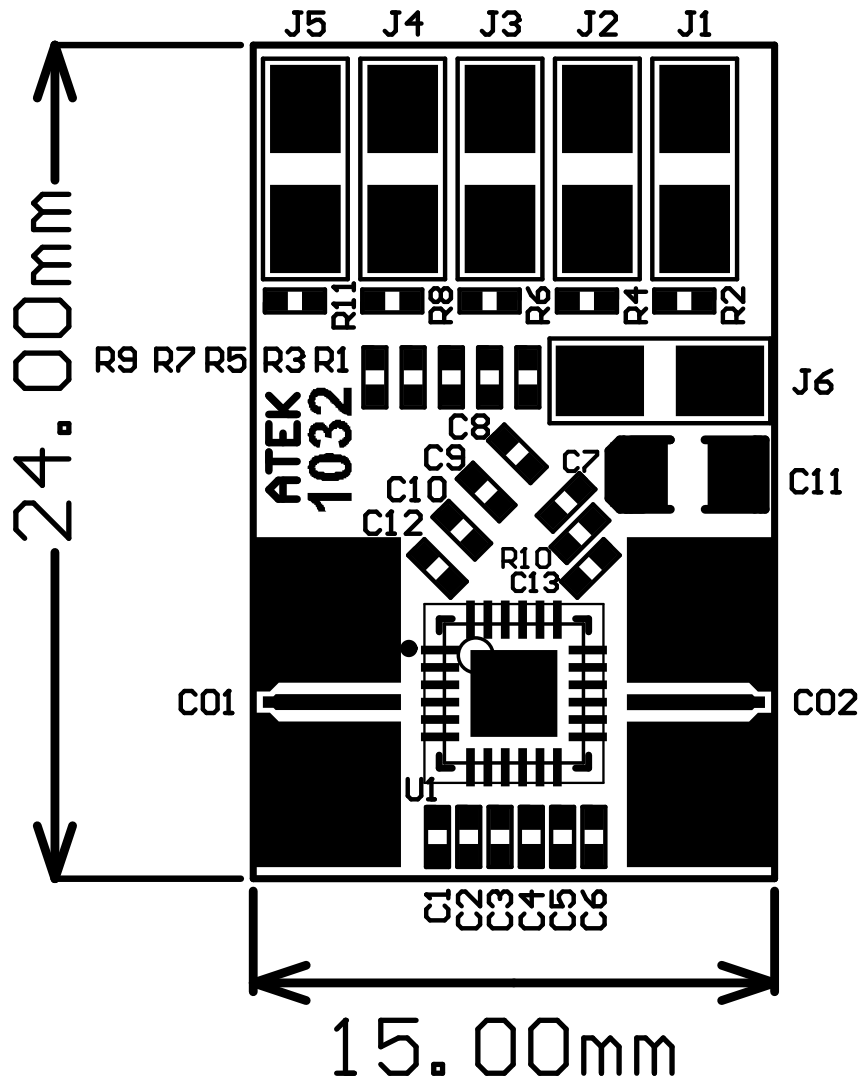
Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	21.03.2022	Initial Release	

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1 GENERAL INFORMATION



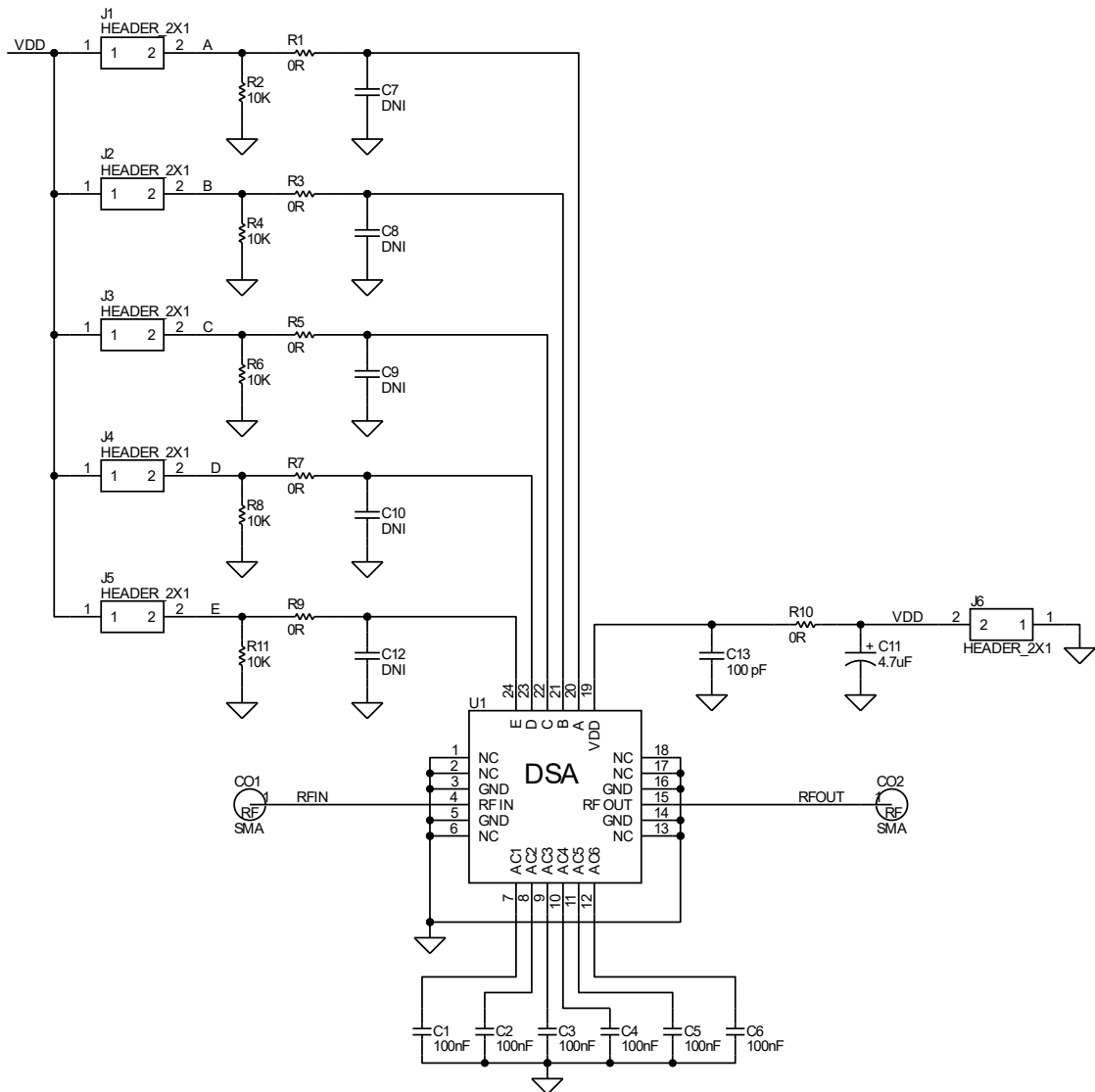
PIN Name	Definition	Comment
C01	RF IN	K Connector
C02	RF OUT	K Connector
J6 Left	VDD	2.54mm Header
J1 Up, J2 Up, J3 Up, J4 Up J5 Up, J6 Right	GND	2.54mm Header
J1 Down	P1 – CTRLA	2.54mm Header
J2 Down	P2 – CTRLB	2.54mm Header
J3 Down	P3 – CTRLC	2.54mm Header
J4 Down	P4 – CTRLD	2.54mm Header
J5 Down	P5 – CTRL E	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltages are detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



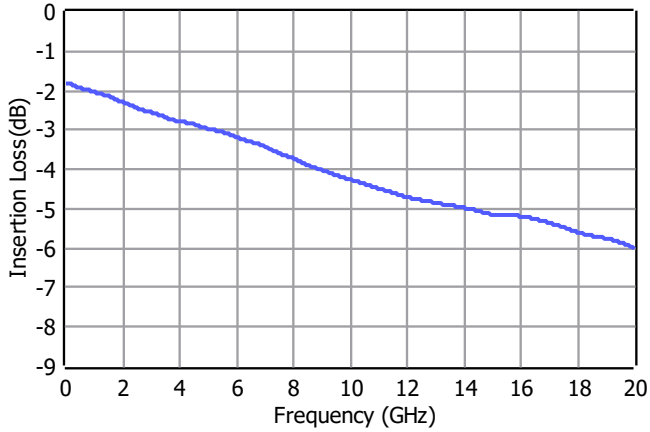
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C2, C3, C4, C5, C6	0402	6	100nF	
C7, C8, C9, C10, C12	0402	5	DNP	
C11	CASEA	1	2.2uF	
C13	0402	1	100pF	
CO1, CO2	K Connector	2	K Connector	ATEK9292
J1, J2, J3, J4, J5, J6	2x1 Header	6	2x1 Header	
R1, R3, R5, R7, R9, R10	0402	6	0R	
R2, R4, R6, R8, R11	0402	5	10k	
U1	ATEKQ4424	1	DSA	ATEK357 P61

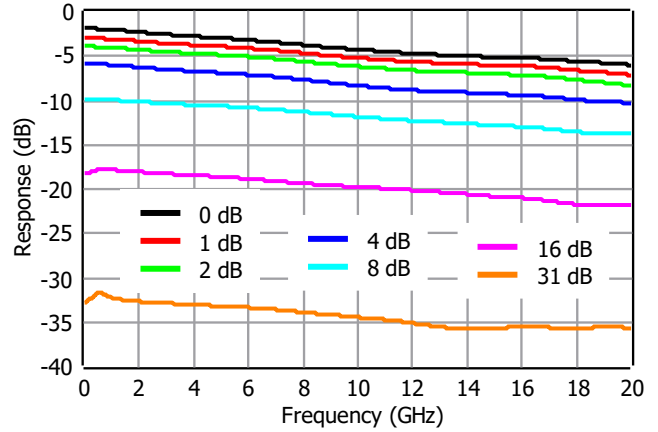
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: $V_{CTRL} = 0/5\text{ V}$, $T = 25\text{ C}$, CW. For details, please refer to the datasheet.

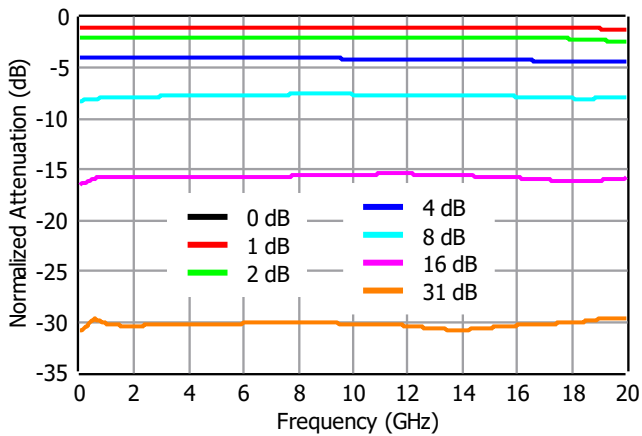
Insertion Loss



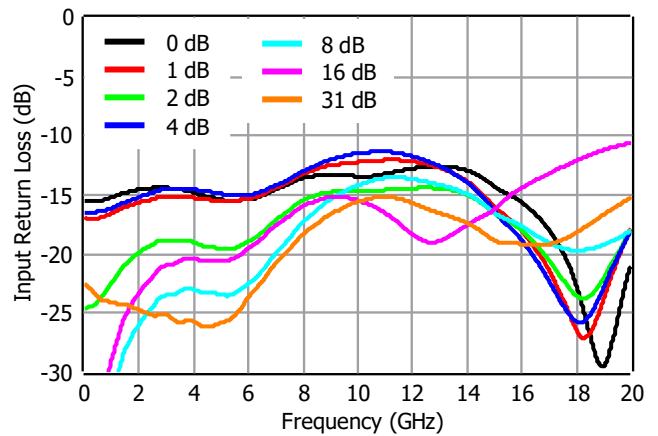
Insertion Loss vs. Attenuation State



Normalized Attenuation



Input Return Loss



Output Return Loss

