



User Guide

EVB-ATEK900N3-01

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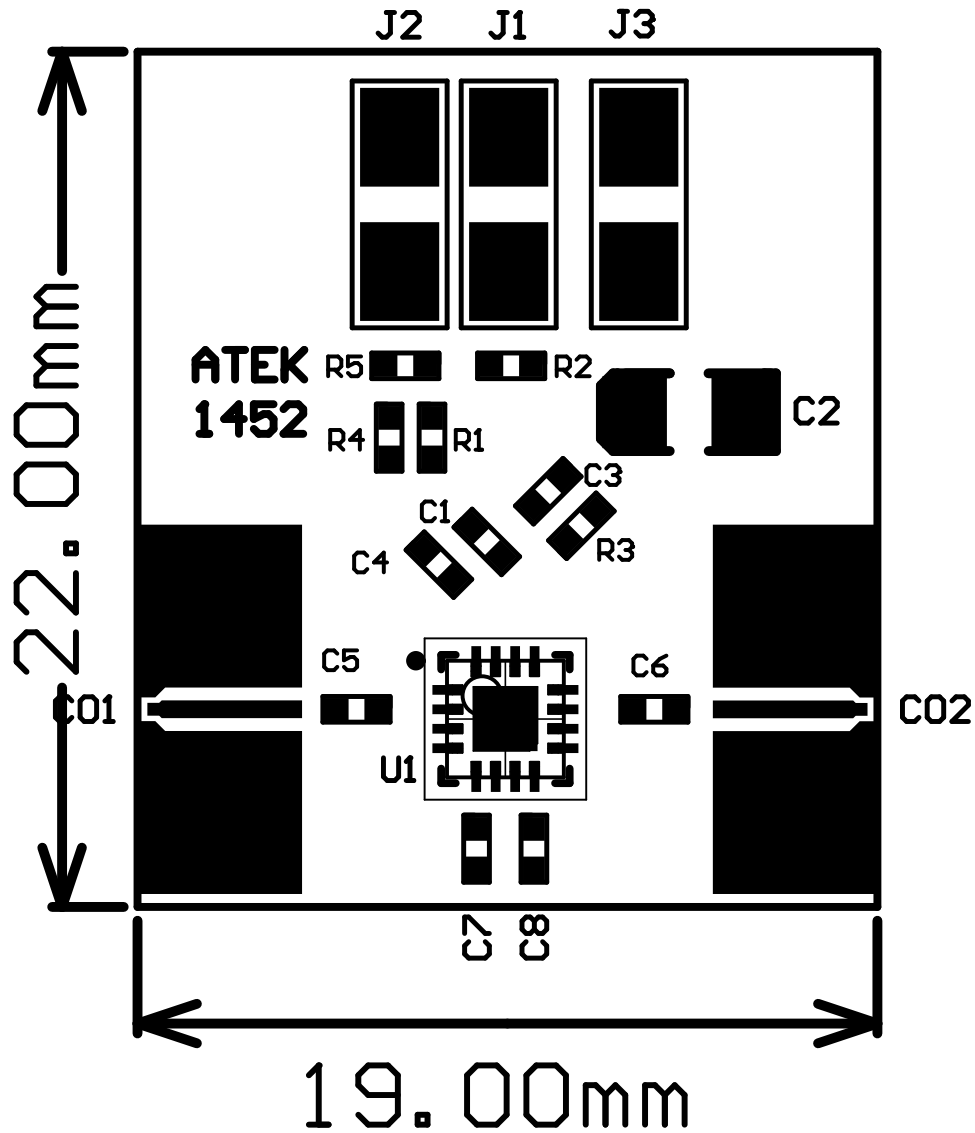
Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	13.03.2022	Initial Release	

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1 GENERAL INFORMATION



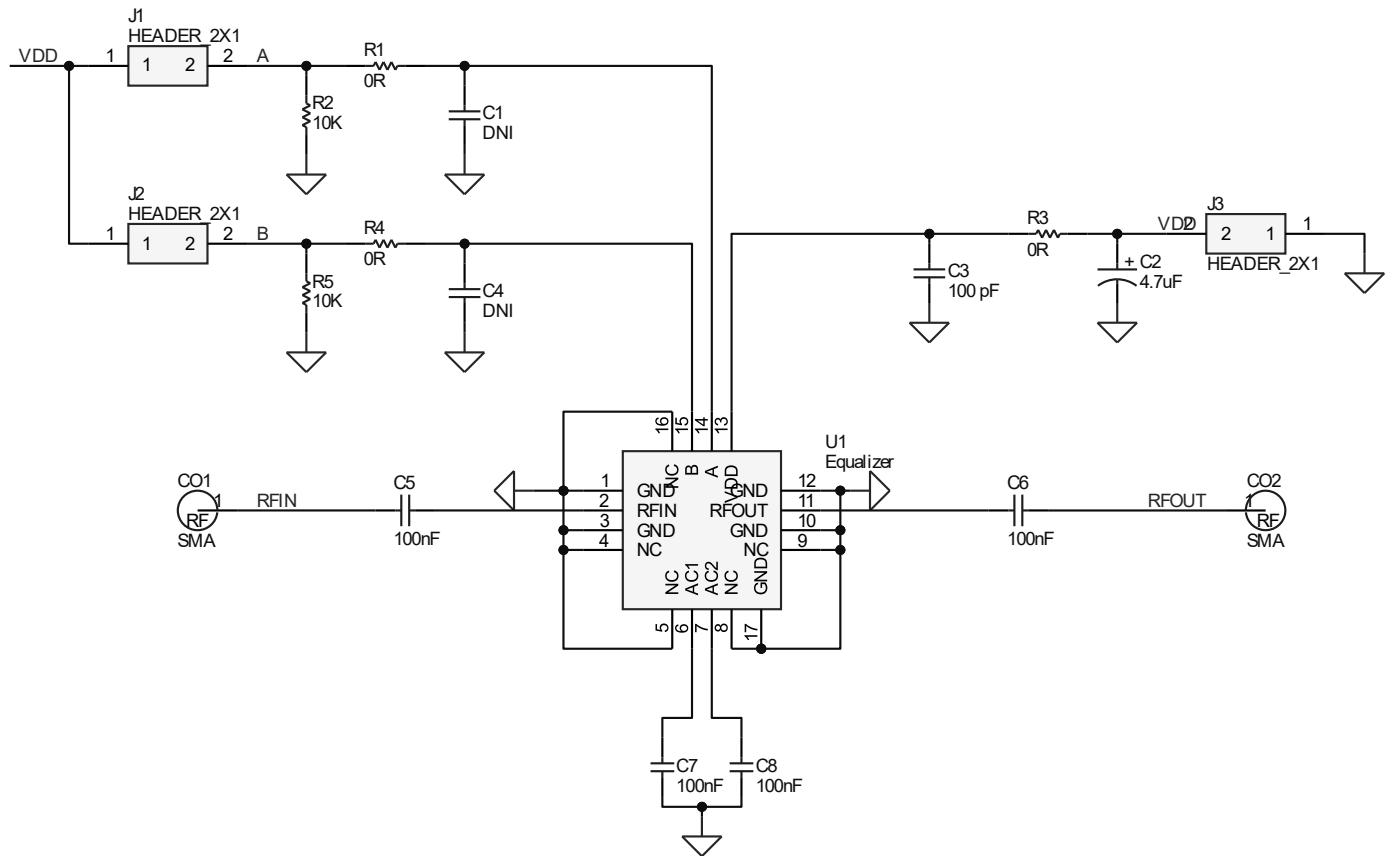
PIN Name	Definition	Comment
CO1	RF IN	K Connector
CO2	RF OUT	K Connector
J1 Up, J2 Up, J3 Down	VDD	2.54mm Header
J1 Down	CTRLB	2.54mm Header
J2 Down	CTRLA	2.54mm Header
J3 Up	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



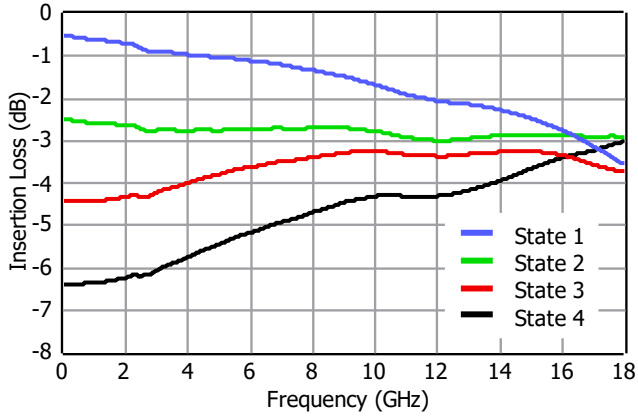
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C4	0402	2	DNP	
C2	CASEA	1	2.2uF	
C3	0402	1	100pF	
C5, C6	0402	2	100nF	530Z104KT10T
C7, C8	0402	2	100nF	
CO1, CO2	K Connector	2	K Connector	ATEK9292
J1, J2, J3	2x1 Header	3	2x1 Header	
R1, R3, R4	0402	3	0R	
R2, R5	0402	2	10k	
U1	ATEKQ3316	1	Equalizer	ATEK900 N60

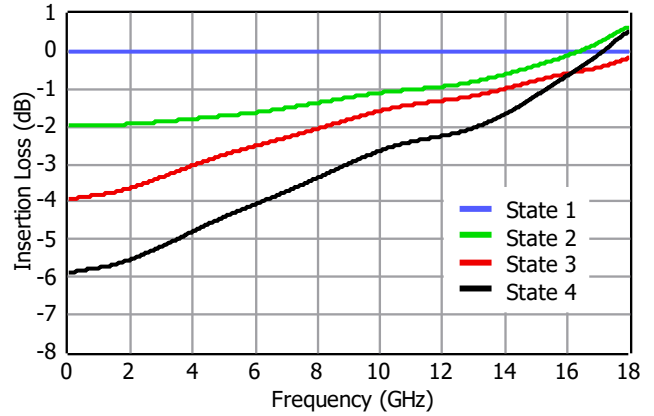
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: $V_{CTRL} = 0/5\text{ V}$, $T = 25\text{ C}$, CW. For details, please refer to the datasheet.

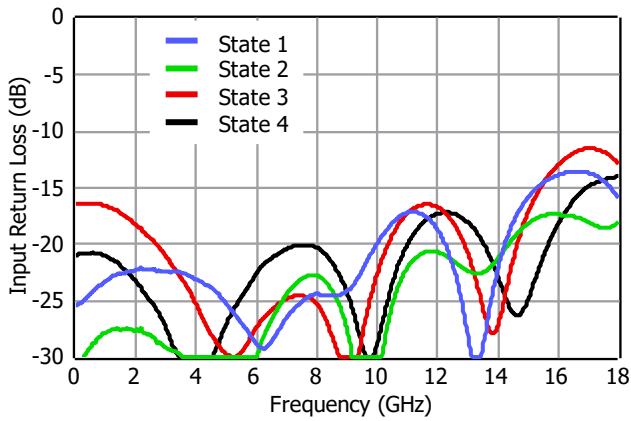
Insertion Loss



Normalized Equalization



Input Return Loss



Output Return Loss

