



User Guide

EVB-ATEK950P6-01

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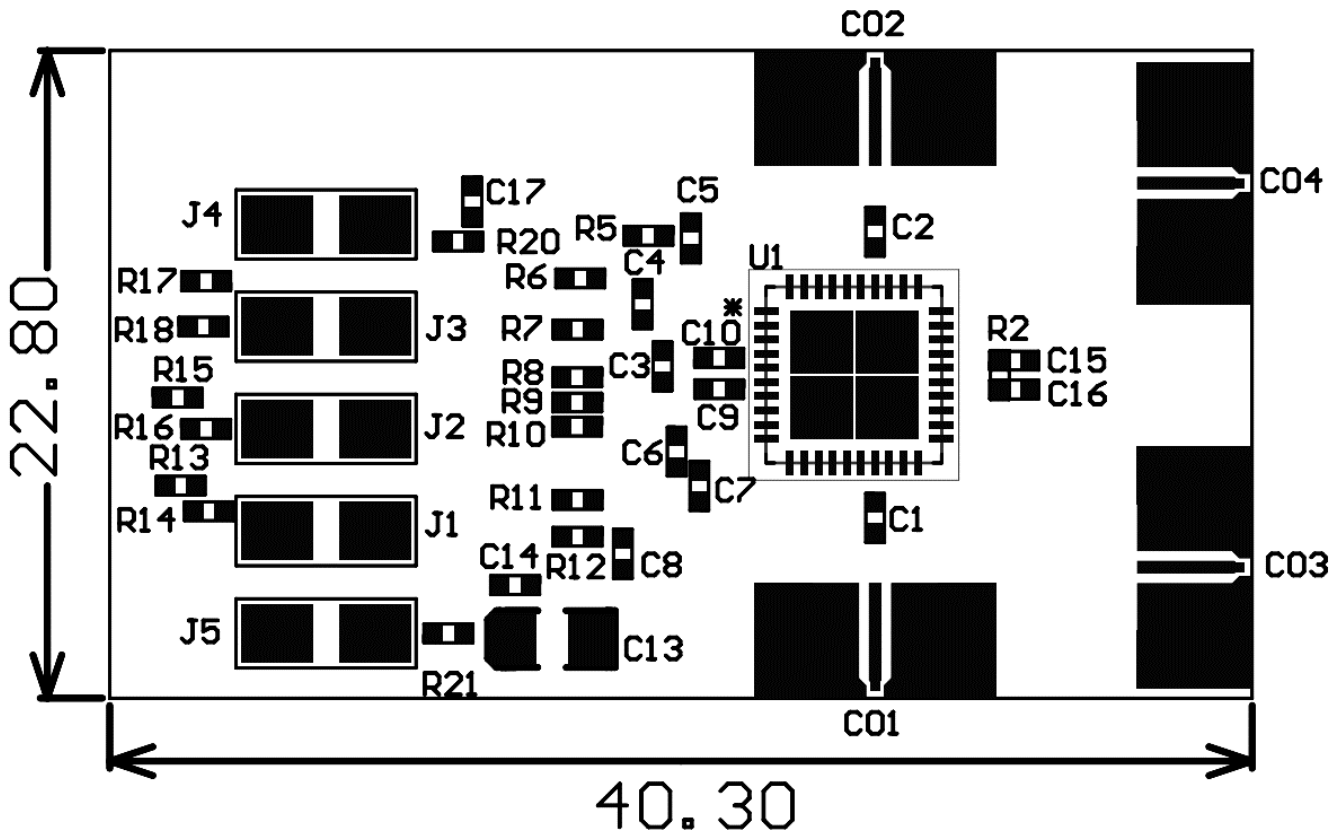
Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	23.03.2022	Initial Release	

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1 GENERAL INFORMATION



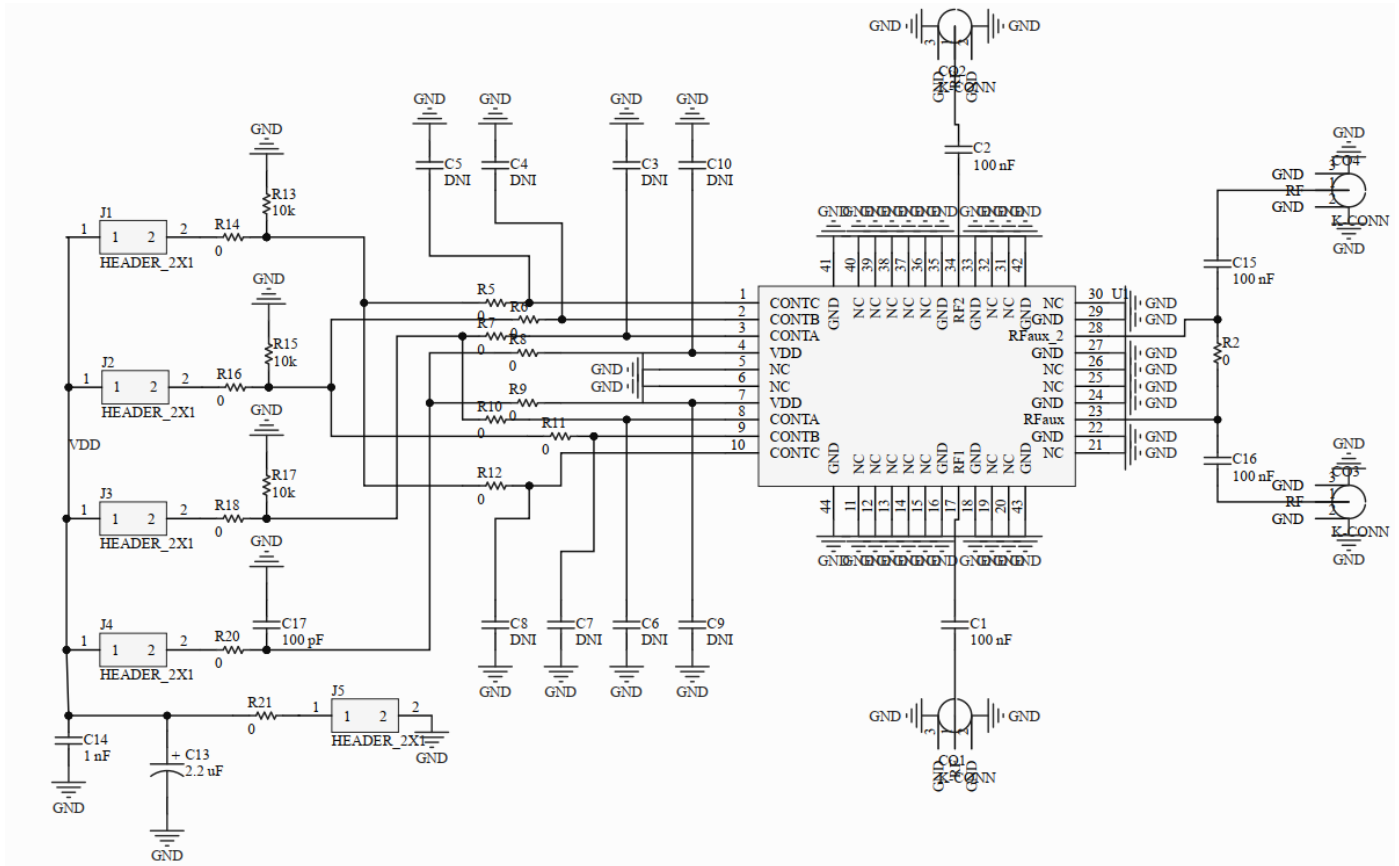
PIN Name	Definition	Comment
C01	RF IN	SMA Connector
C02	RF OUT	SMA Connector
C03, C04	ByPass Path / RF Aux	SMA Connector
J1 Right, J2 Right, J3 Right	N/A	2.54mm Header
J1 Left	CTRL C	2.54mm Header
J2 Left	CTRL B	2.54mm Header
J3 Left	CTRL A	2.54mm Header
J4 Right, J4 Left	Shorted	2.54mm Header
J5 Right	VDD	2.54mm Header
J5 Left	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. CTRL A, CTRL B and CTRL C are detailed in Datasheet.
3. The definition of right and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



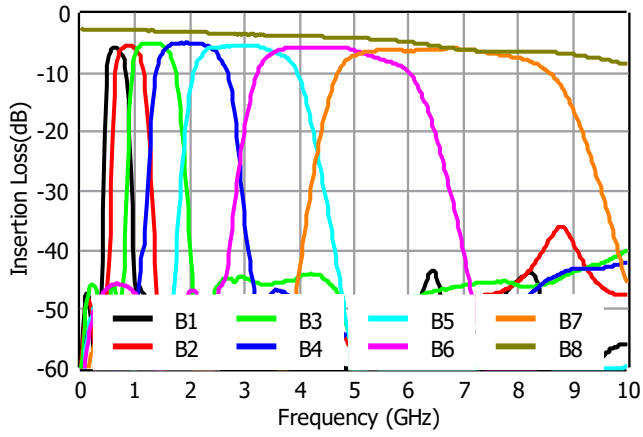
2.2 BOM

Designator	Footprint	Qty	Comment	PN
C1, C2, C15, C16	0402	4	100nF	
C3, C4, C5, C6, C7, C8, C9, C10	0402	8	DNP	
C13	CASEA	1	2.2uF	
C14	0402	1	1nF	
C17	0402	1	100pF	
CO1, CO2, CO3, CO4	SMA Connector	4	SMA Connector	
J1, J2, J3, J4, J5	2x1 Header	5	2x1 Header	
R2	0402	1	DNP	
R5, R6, R7, R8, R9, R10, R11, R12, R14, R16, R18, R20, R21	0402	13	0R	
R13, R15, R17	0402	3	10k	
U1	ATEKQ6640	1	Filter Bank	ATEK950P6

3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: $V_{CTRL} = 0/5\text{ V}$, $T = 25\text{ C}$, CW. For details, please refer to the datasheet.

S21, Vdd=5V



S21, Vdd=5 V, Log Scale

