

# User Guide

## EVB-ATEK951P4-01

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**Revisions**

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	28.07.2021	Initial Version	

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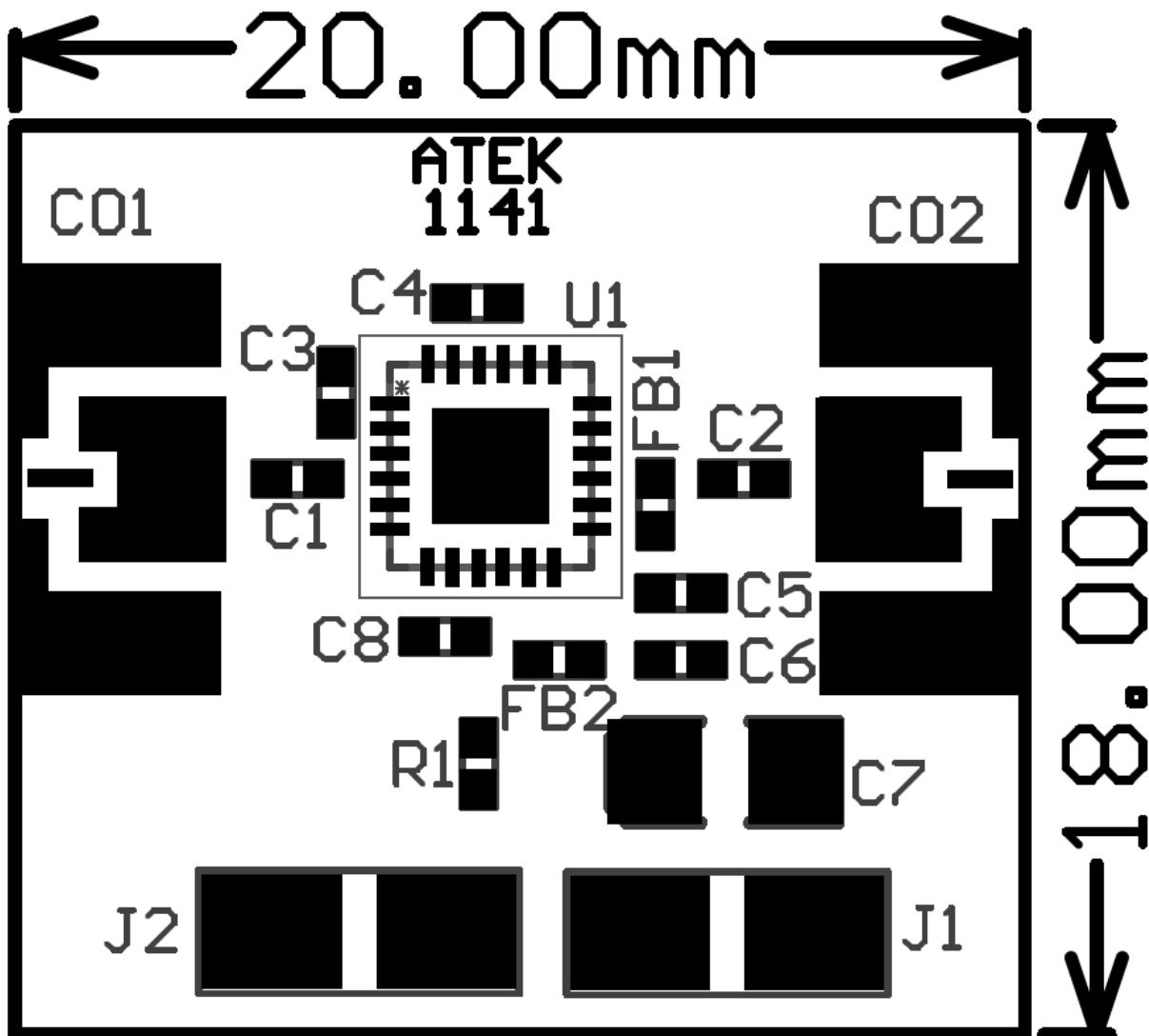
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1 GENERAL INFORMATION



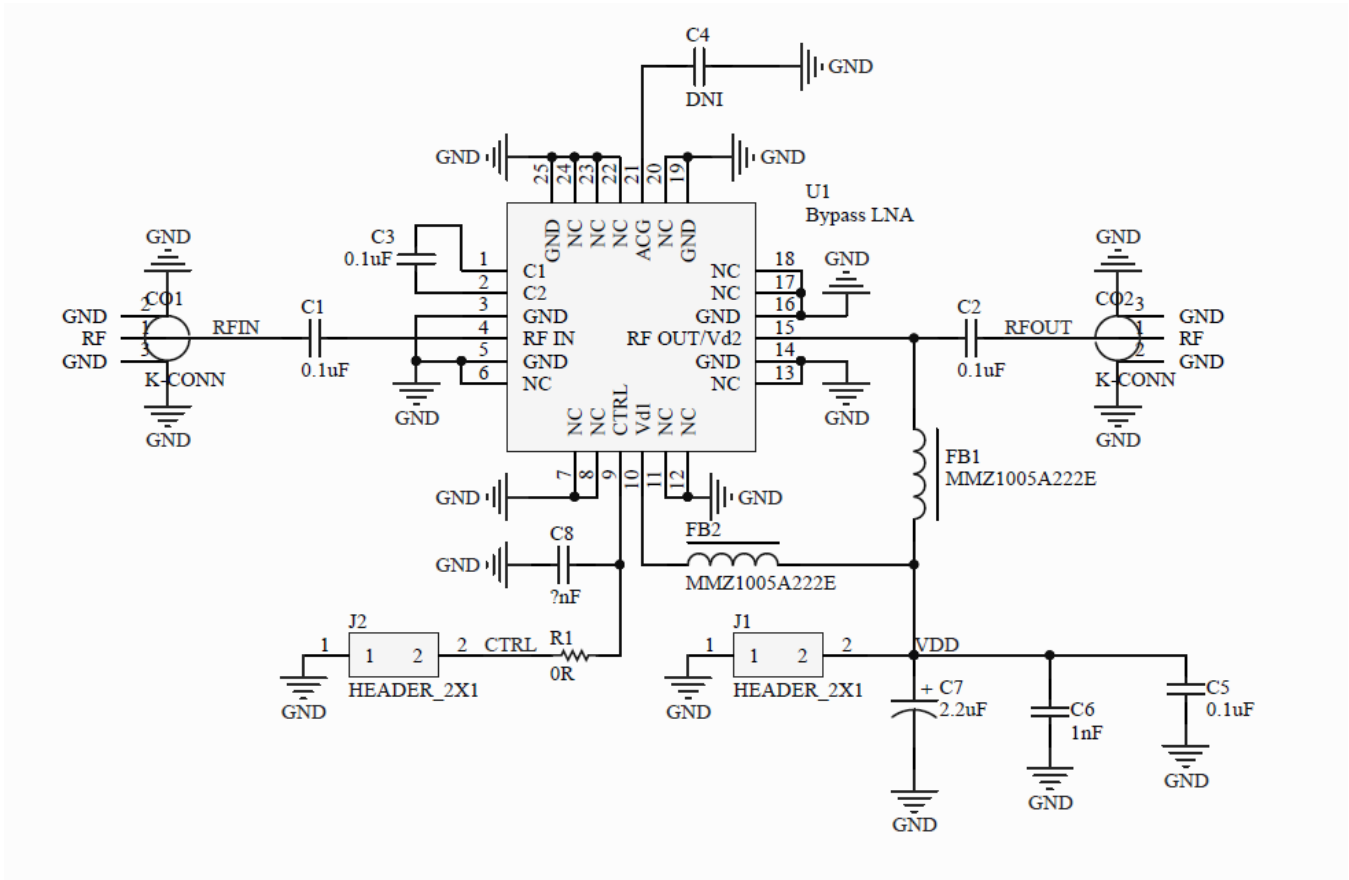
PIN Name	Definition	Comment
<b>CO1</b>	RF IN	SMA Connector
<b>CO2</b>	RF OUT	SMA Connector
<b>J1 Right</b>	GND	2.54mm Header
<b>J1 Left</b>	VDD	2.54mm Header
<b>J2 Right</b>	Control Voltage	2.54mm Header
<b>J2 Left</b>	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. Control Voltage is detailed in Datasheet.
3. The definition of up, down, right, and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



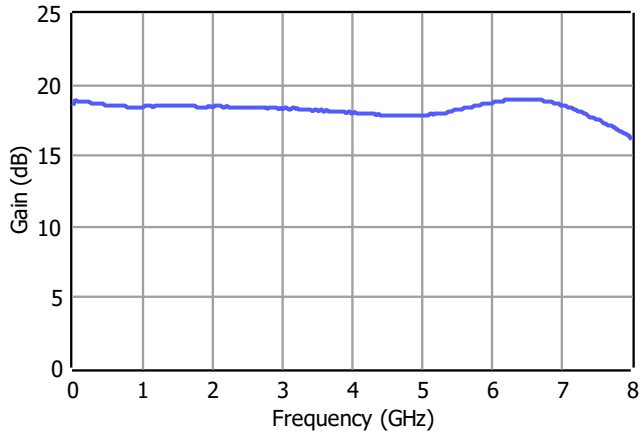
2.2 BOM

Designator	Footprint	Qty	Comment	PN
<b>C1, C2, C3</b>	0402	3	0.1uF	530Z104KT10T
<b>C4</b>	0402	1	DNP	
<b>C5</b>	0402	1	0.1uF	
<b>C6</b>	0402	1	1nF	
<b>C7</b>	CASEA	1	2.2uF	
<b>C8</b>	0402	1	DNP	
<b>CO1, CO2</b>	SMA Connector	2	SMA Connector	
<b>FB1, FB2</b>	0402	2	Ferrite Bead	MMZ1005A222E
<b>J1, J2</b>	HEADER_2X1_V2	2	HEADER_2X1	
<b>R1</b>	0402	1	OR	
<b>U1</b>	ATEKQ4424	1	Bypass LNA	ATEK951 P46

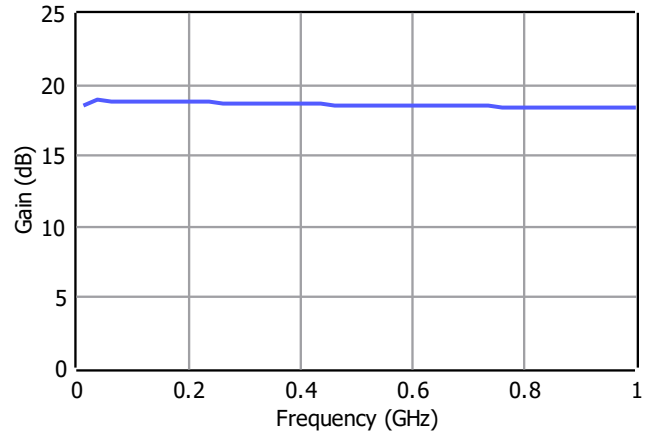
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified:  $V_{dd} = 5\text{ V}$ ,  $T = 25\text{ C}$ , CW. For details, please refer to the datasheet.

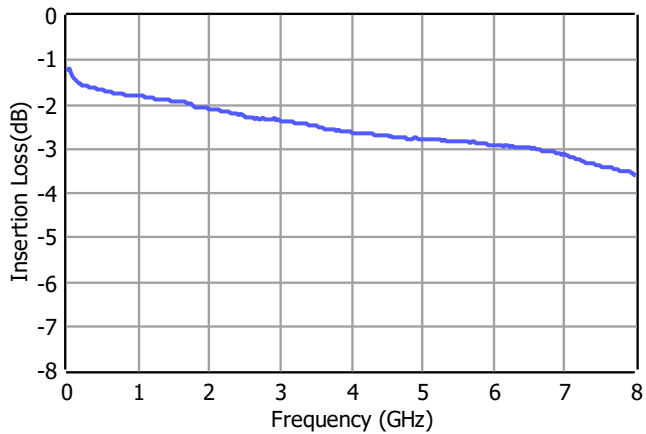
Gain Wideband, LNA State



Gain Low Frequency, LNA State



Insertion Loss WideBand, Bypass State



Insertion Loss Low Frequency, Bypass State

