

Product Description

ATEK252N3 is a wideband absorptive SPDT switch with low loss and high isolation. Frequency of operation starts from low frequencies close to DC, goes up to 24 GHz.

RF input, outputs are matched to 50 ohms internally. Switch is housed in a compact low cost 3x3 mm surface mount package.

Evaluation Board, bare die, custom package, and module options are available upon request.

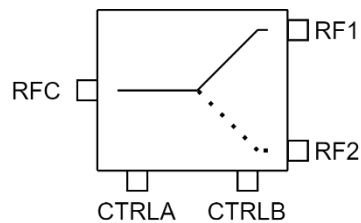
Product Features

- Frequency Range: LF - 24 GHz
- Insertion Loss: 2 dB at 20 GHz
- IP1dB: 25 dBm @ 10 GHz
- IIP3: 46 dBm @ 10 GHz
- 3x3 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test and Measurement
- Radar
- Electronic Warfare

Functional Block Diagram



Electrical Specifications

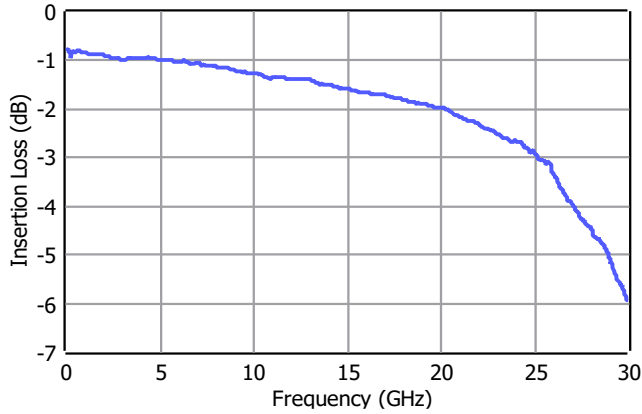
Conditions unless otherwise specified: T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		LF		24	GHz
Insertion Loss	2 GHz		0.9		dB
	10 GHz		1.3		
	15 GHz		1.6		
	20 GHz		2		
	24 GHz		2.7		
Isolation	2 GHz		66		dB
	10 GHz		59		
	15 GHz		51		
	20 GHz		59		
	24 GHz		47		
Input Return Loss			17		dB
Output Return Loss			17		dB
Input P1dB			25		dBm
Input IP3			45		dBm
Switching Time	On		4		ns
	Off		45		
Control Voltage (CTRL)	Low	0			V
	High			-5	
Operating Temperature		-40		85	°C

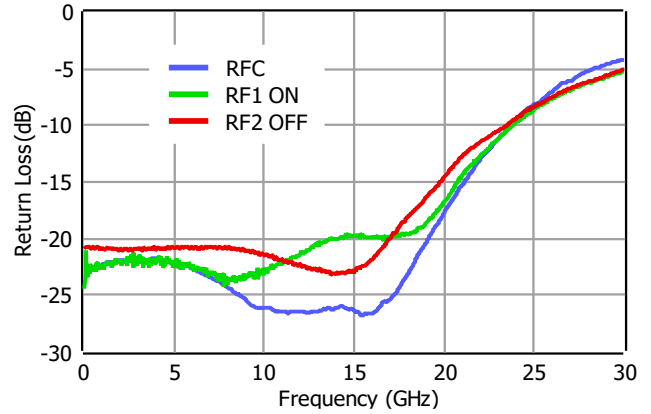
Typical Performance Plots

Conditions unless otherwise specified: T = 25 C, CW.

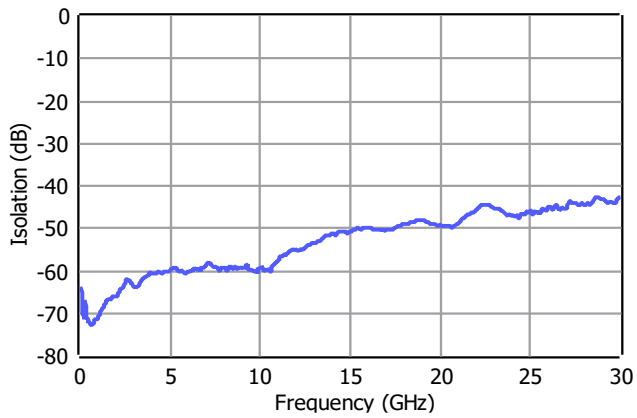
Insertion Loss



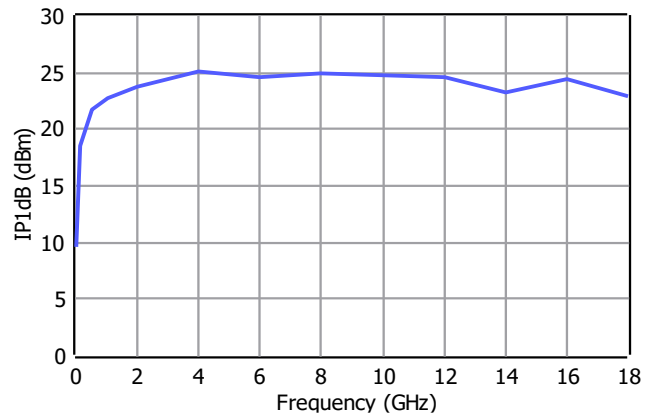
Return Loss



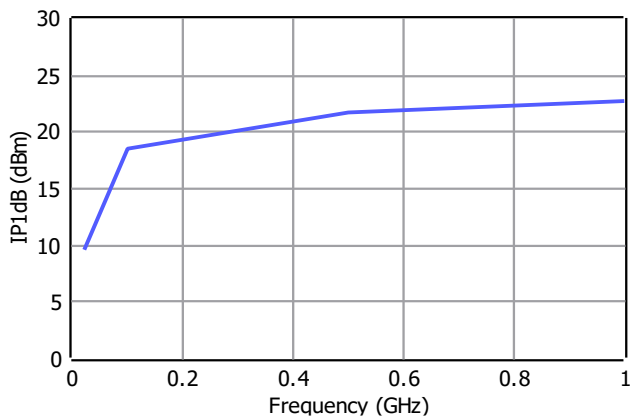
Isolation from RFC to RF2



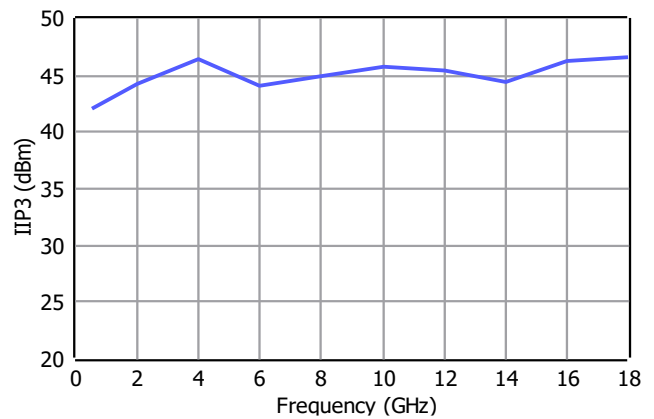
Input P1dB Wideband



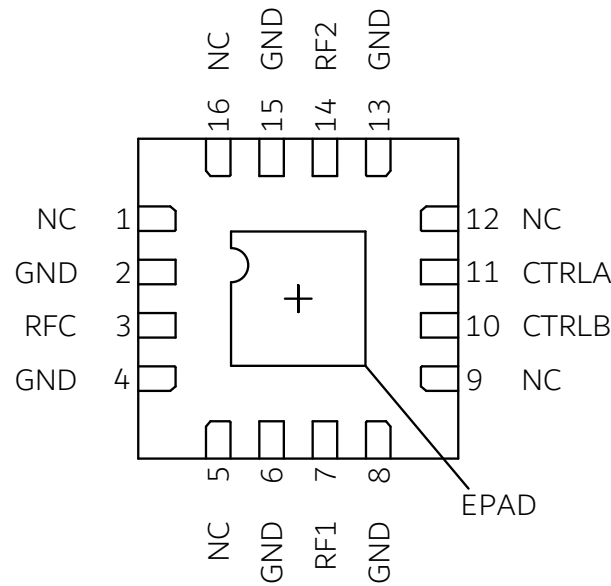
Input P1dB Low Frequency



Input IP3



Pin Description



Pin Number	Pin Name	Description
3	RFC	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
7	RF1	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
14	RF2	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
10	CTRLB	Control pin.
11	CTRLA	Control pin.
1, 5, 9, 12, 16	NC	These pins are not internally connected. Can be grounded on the PCB.
2, 4, 6, 8, 13, 15	GND	Ground.
17	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

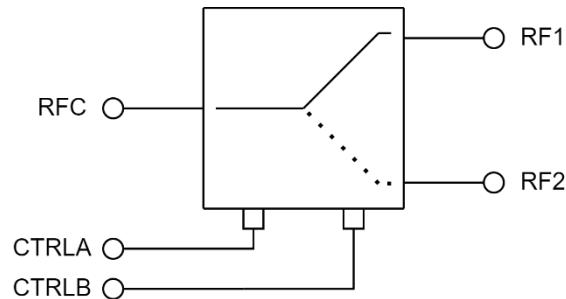
Control Interface

CTRLA	CTRLB	RFC to RF1	RFC to RF2
HIGH	LOW	ON	OFF
LOW	HIGH	OFF	ON

Applications Information

Signal entering from RFC goes to RF1 or RF2 depending on the switch state set by the user. Switch is bi-directional. Switch state can be set by switching control voltages between 0 V to -5 V.

Typical application schematic to operate the SPDT switch is given below.



CTRLA and CTRLB signals are used for setting the switch state.

If needed, to filter out the ripples and unwanted signals on the external CTRL signals, a low pass filter in series R, shunt C configuration can be implemented on the CTRL lines. Note that external RC filtering limits the state switching speed of the SPDT.

All datasheet plots are generated by an evaluation board (EVB) with the application schematic provided above. For s-parameters measurements, RF lines on the EVB are connected to the RF pins of the SPDT, then RF lines are probed with an RF probe to perform the measurements.

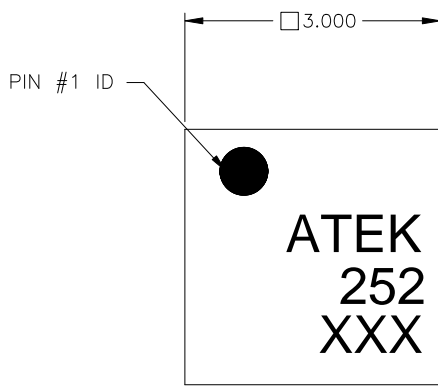
NC pins of the SPDT are connected to the GND on the EVB used to generate the plots shown in this document.

Absolute Maximum Ratings

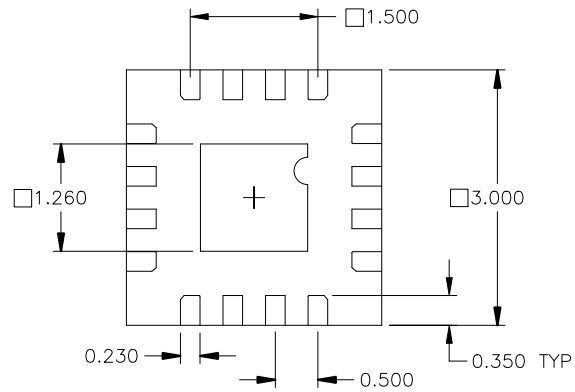
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	-55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

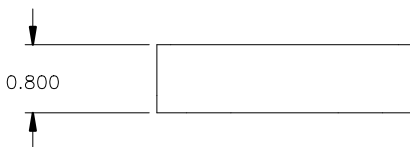
Mechanical and Marking Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTES

1. JEDEC OUTLINE: MO-220
2. ALL DIMENSIONS IN MM
3. TOLERANCE IN X.XX= ± 0.15 X.XXX= ± 0.050

Handling Precautions



Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	22.06.2021	Initial Version	
1.1	05.07.2021	Drawing and Plots Revised	3/7, 6/7