Product Description

ATEK359P4 is a 5-bit Digital Step Attenuator with 31 dB attenuation range. Attenuator frequency of operation goes down to 500 MHz and goes up to 4 GHz.

Bias and control voltages of the attenuator are positive, which eliminates the need for negative voltage rails.

Attenuator is housed in compact 4x4 mm low cost SMD package, input and output matched to 50 ohms internally.

Evaluation Board, bare die, custom package, and module options are available upon request.

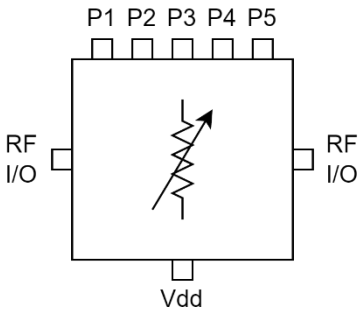
Product Features

- Frequency Range: 0.5 - 4 GHz
- Insertion Loss: 1.8 dB at 2.4 GHz
- Attenuation Range: 31.5 dB at 2.4 GHz
- Positive Supply
- Positive Control
- 4x4 mm compact size

Applications

- Wideband Receivers
- Telecommunication
- Test Equipment
- SDR
- Positioning

Functional Block Diagram



Electrical Specifications

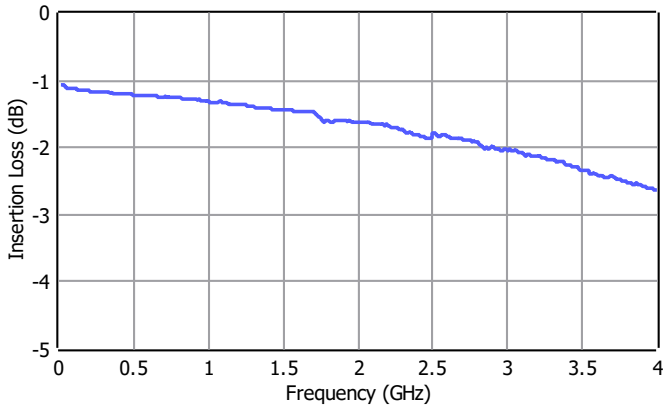
Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.5		4	GHz
Insertion Loss	0.5 GHz		1.2		dB
	1 GHz		1.3		
	2 GHz		1.6		
	3 GHz		2.1		
	4 GHz		2.6		
Attenuation Range	0.5 GHz		30.5		dB
	1 GHz		31.5		
	2 GHz		31.5		
	3 GHz		31		
	4 GHz		30.5		
State Error			0.6		dB
Input Return Loss			-15		dB
Output Return Loss			-15		dB
Input P1dB			TBD		dBm
Input IP3			TBD		dBm
Switching Time	On		TBD		ns
	Off		TBD		
DC Supply Voltage (Vdd)			5		V
DC Supply Current			5		mA
Control Voltage (P1-5)	Low		0		V
	High		Vdd		
Operating Temperature		-40		85	°C

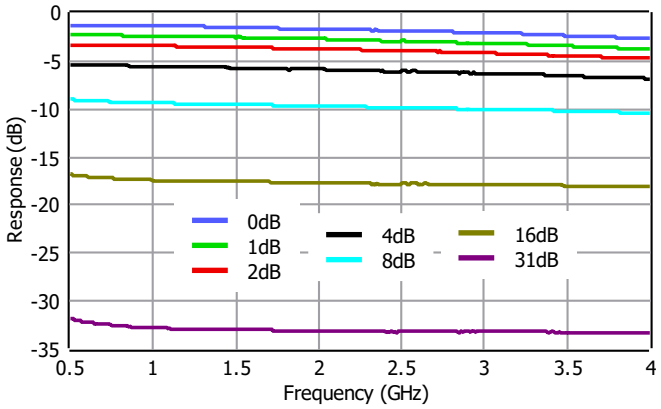
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

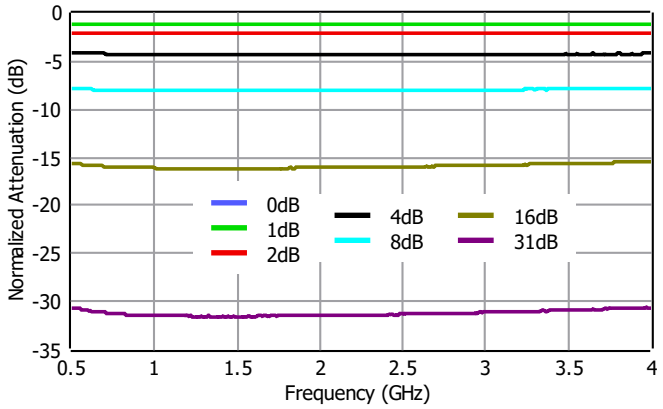
Insertion Loss



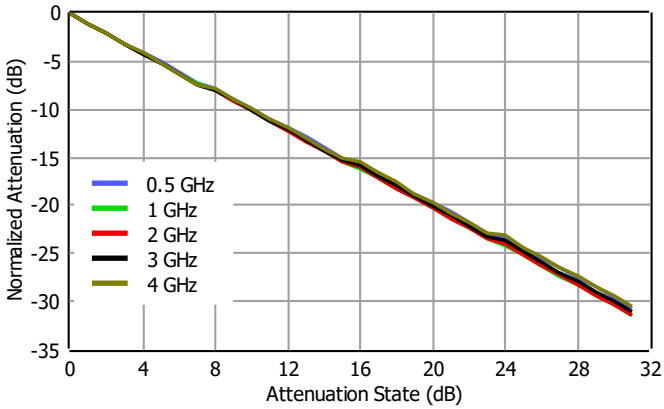
Insertion Loss vs. Attenuation State



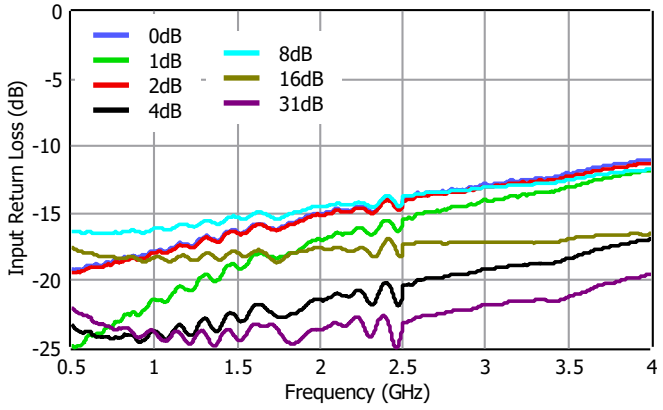
Normalized Attenuation



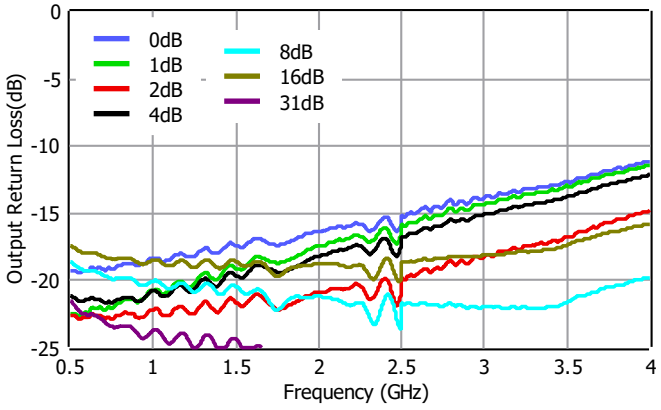
Normalized Attenuation vs. Attenuation State, Frequency



Input Return Loss



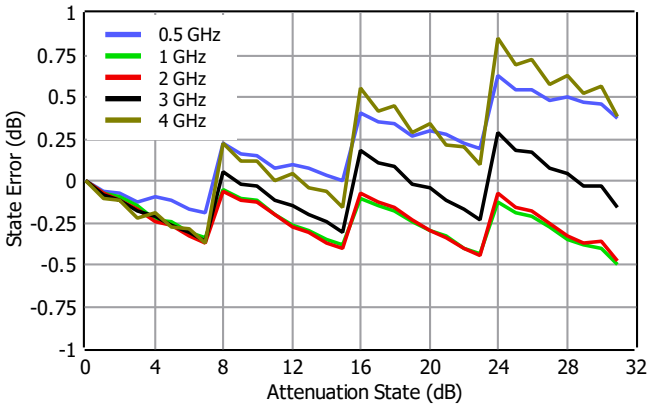
Output Return Loss



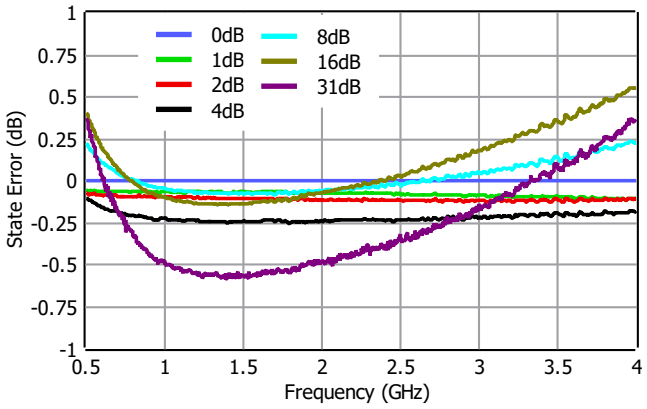
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, Typical, T = 25 C, CW.

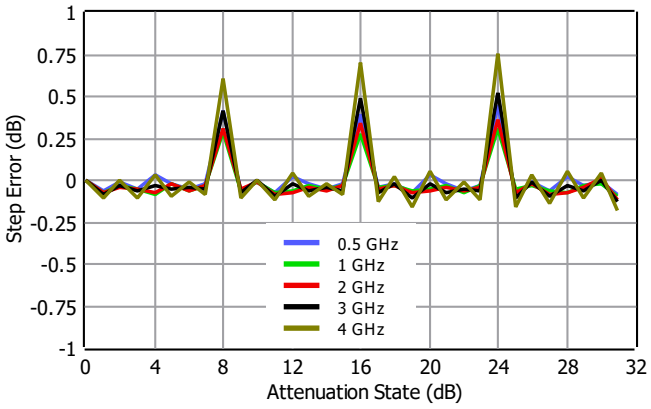
State Error vs. Attenuation State, Frequency



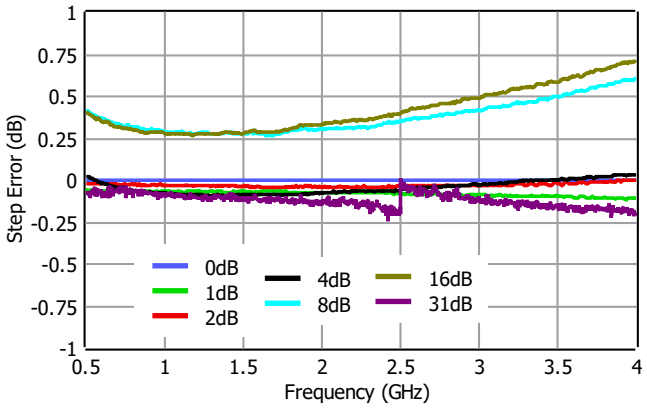
State Error vs. Attenuation State



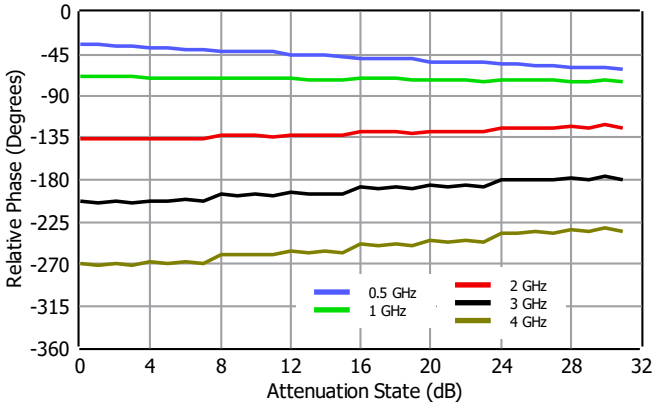
Step Error vs Attenuation State, Frequency



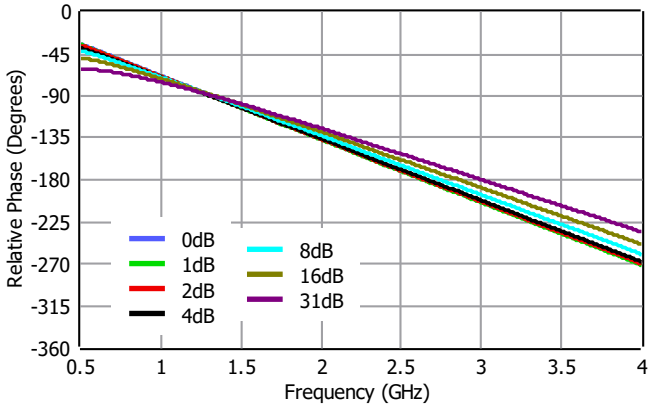
Step Error vs. Attenuation State



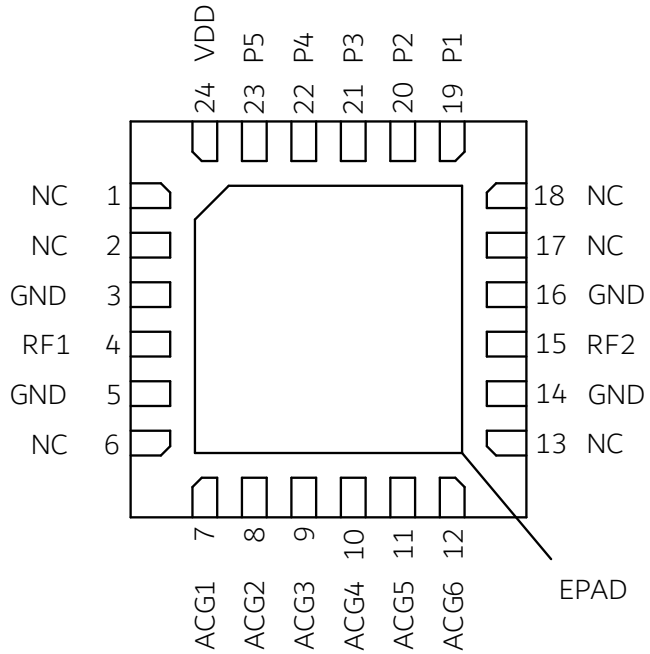
Relative Phase vs. Attenuation State, Frequency



Relative Phase vs. Attenuation State



Pin Description



Top View

Pin Number	Pin Name	Description
4	RF1	RF input/output pin. DC block capacitor is required.
15	RF2	RF input/output pin. DC block capacitor is required.
24	VDD	Vdd bias pin.
19	P1	Control voltage pin for parallel control interface.
20	P2	Control voltage pin for parallel control interface.
21	P3	Control voltage pin for parallel control interface.
22	P4	Control voltage pin for parallel control interface.
23	P5	Control voltage pin for parallel control interface.
7	ACG1	AC ground pin. External shunt capacitor is required.
8	ACG2	AC ground pin. External shunt capacitor is required.
9	ACG3	AC ground pin. External shunt capacitor is required.
10	ACG4	AC ground pin. External shunt capacitor is required.
11	ACG5	AC ground pin. External shunt capacitor is required.
12	ACG6	AC ground pin. External shunt capacitor is required.
1, 2, 6, 13, 17, 18	NC	These pins are not internally connected. Can be grounded on the PCB.
3, 5, 14, 16	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

Control Interface

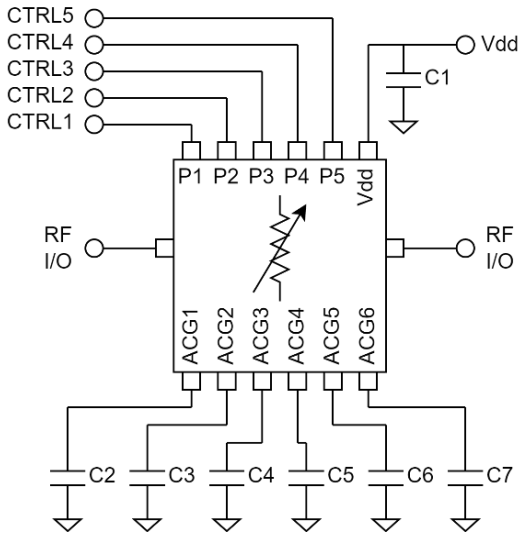
P5	P4	P3	P2	P1	Attenuation State
LOW	LOW	LOW	LOW	LOW	0 dB
LOW	LOW	LOW	LOW	HIGH	1 dB
LOW	LOW	LOW	HIGH	LOW	2 dB
LOW	LOW	HIGH	LOW	LOW	4 dB
LOW	HIGH	LOW	LOW	LOW	8 dB
HIGH	LOW	LOW	LOW	LOW	16 dB
HIGH	HIGH	HIGH	HIGH	HIGH	31 dB

Applications Information

Signal entering from RF IN goes to RF OUT with an attenuation level set by control pins.

Vdd bias is 5 V and control voltages are CMOS compatible. Attenuation level can be set by switching control voltages between 0 V to 5 V. Operating the attenuator is done with positive voltage rails without the need for negative voltage levels.

Typical application schematic to operate the attenuator is given below.



C1 is used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C1 will improve this filtering. If this filtering is of no concern, then attenuator can be operated without C1.

If needed, to filter out the ripples and unwanted signals on the external CTRL signal, a low pass filter in series R, shunt C configuration can be implemented on the CTRL line. Note that external RC filtering limits the attenuation switching speed of the attenuator.

CTRL1-5 voltages are used for setting the attenuation level.

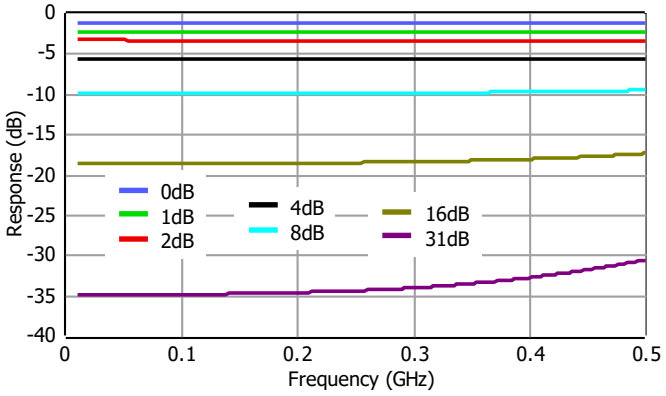
All measurement results presented on this document are taken with a set-up, where RF1 is an input and RF2 is an output.

C2, C3, C4, C5, C6 and C7 are AC ground capacitors. Measurement in this document generated without ACG capacitors. Values of these capacitors should be chosen considering the lowest operation frequency of the application. Insertion Loss, Attenuation and IP3 performance is measured with connectorized evaluation PCB. Then the loss of the PCB is de-embedded to generate the data presented in this document.

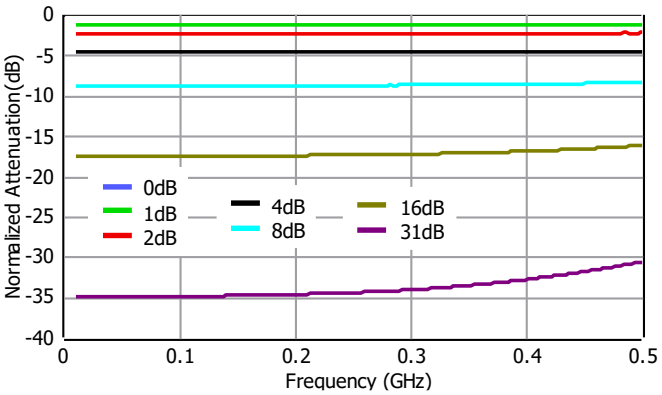
The NC pins of the attenuator are connected to the GND on the PCB used to generate the plots shown in this document.

100 nF is installed to C2-C7 ACG capacitors to generate the measurement results shown below for low frequency applications covering 10 MHz – 500 MHz.

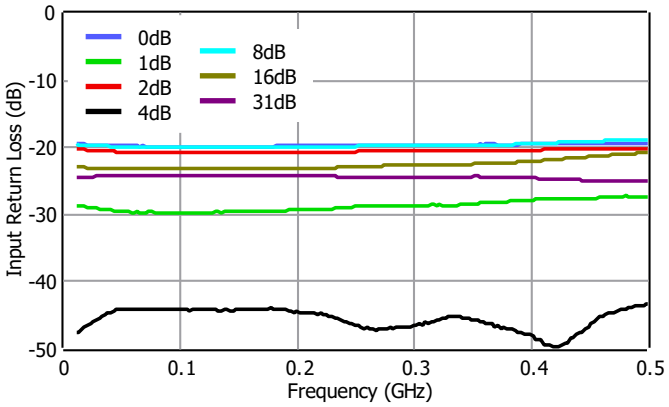
Insertion Loss vs. Attenuation State



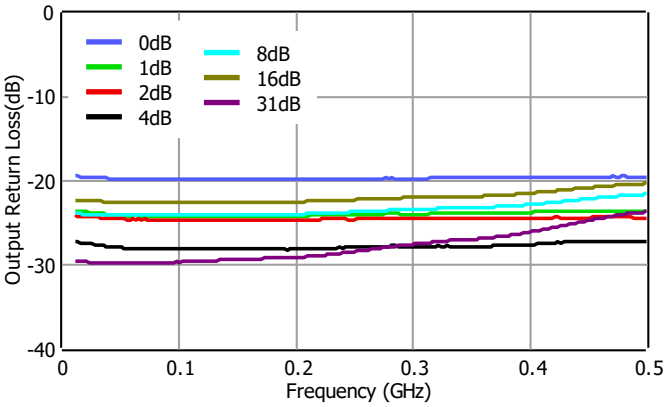
Normalized Attenuation



Input Return Loss



Output Return Loss

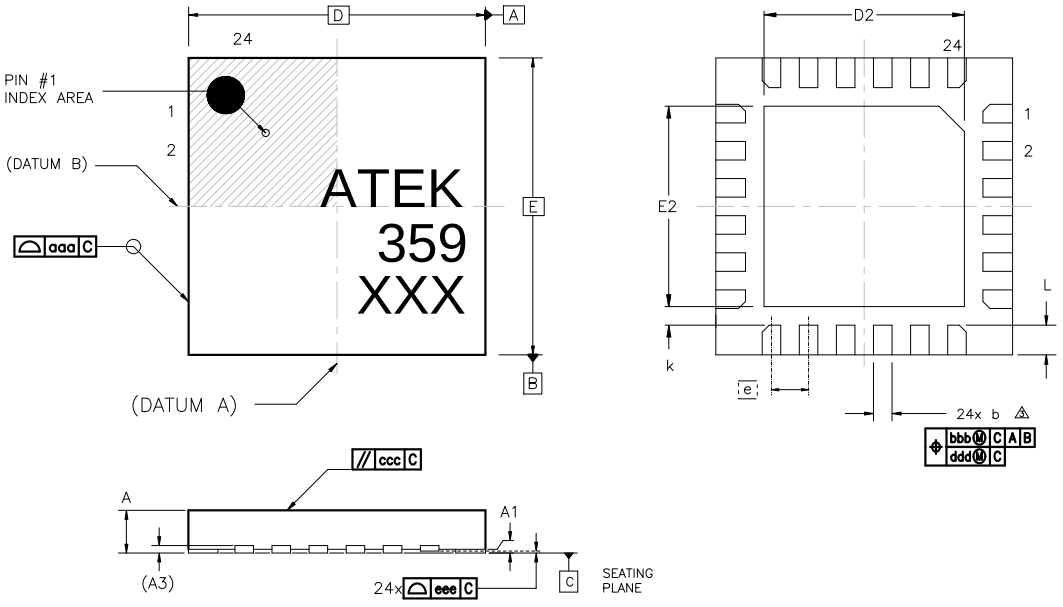


Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltage (Vdd)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These conditions should not be applied simultaneously.

Mechanical and Marking Information



NOTES:
1) ALL DIMENSIONS IN MM
2) DIMENSIONING AND TOLERANCING PER ASME Y14.5–2009
3) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
A, W	0.70	0.80	e	0.50 BSC	
A, L	1.40	1.70	k	0.20	–
A1	0.00	0.05	L	0.35	0.45
A3	0.20 REF		aaa	0.10	
b	0.18	0.30	bbb	0.10	
D	4.00 BSC		ccc	0.10	
D2	2.60	2.80	ddd	0.05	
E	4.00 BSC		eee	0.08	

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	18.10.2022	Initial Release	