Product Description

ATEK951P4 is a wideband low noise amplifier with bypass option covering 0.01 to 8 GHz frequency range. Amplifier operational low frequency range can be extended to lower frequencies by increasing external component values.

Amplifier provides flat gain and low noise over wideband with single supply voltage. Bypass state is controlled with positive voltage, eliminating the need for negative voltage rails. This allows users to easily realize wideband receiver frontends.

Amplifier housed in compact 4x4 mm low cost SMD package, input and output matched to 50 ohms internally.

Evaluation Board, bare die, custom package, and module options are available upon request.

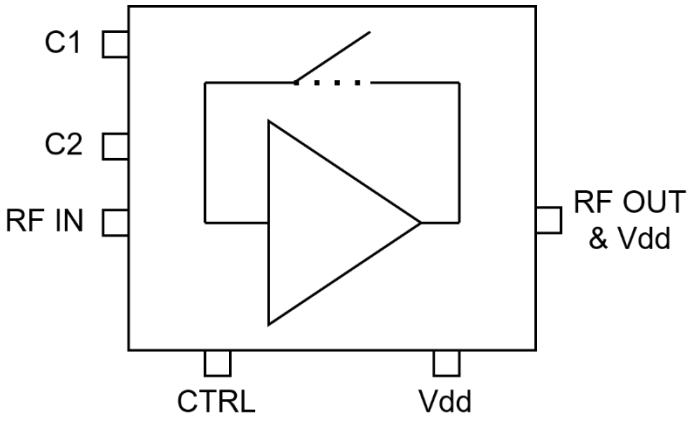
Product Features

- Frequency Range: 0.01 - 8 GHz
- Gain: 18 dB
- Noise Figure: 2.5 dB
- P1dB: 17 dBm
- Single Supply
- Positive Control
- 4x4 mm compact size

Applications

- Wideband Receivers
- SDR
- Test Equipment
- Radar
- Electronic Warfare
- COMINT
- Telecommunication

Functional Block Diagram



Electrical Specifications

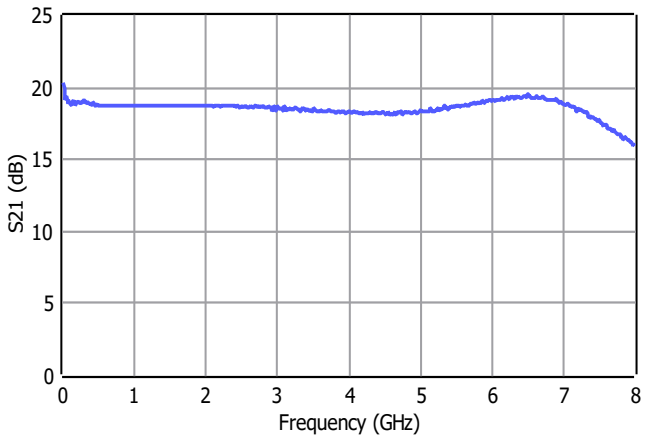
Conditions unless otherwise specified: V_{DD} = 5 V, T = 25 C, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		0.01		8	GHz
Gain	0.01 GHz		19		dB
	1 GHz		18		
	3 GHz		18		
	6 GHz		19		
	8 GHz		16.5		
Noise Figure	0.01 GHz		6		dB
	1 GHz		2.5		
	3 GHz		2		
	6 GHz		2.8		
	8 GHz		4.5		
Input Return Loss			-11		dB
Output Return Loss			-12		dB
Bypass State Insertion Loss			2.5		dB
Bypass State Input Return Loss			-16		dB
Bypass State Output Return Loss			-16		dB
Output IP3			30		dBm
Output P1dB			17		dBm
DC Supply Voltage (Vdd)			5		V
DC Supply Current	LNA State		82		mA
	Bypass Sate		5		
Control Voltage (CTRL)	Low	0		1	V
	High	2		5	
Operating Temperature		-40		85	°C

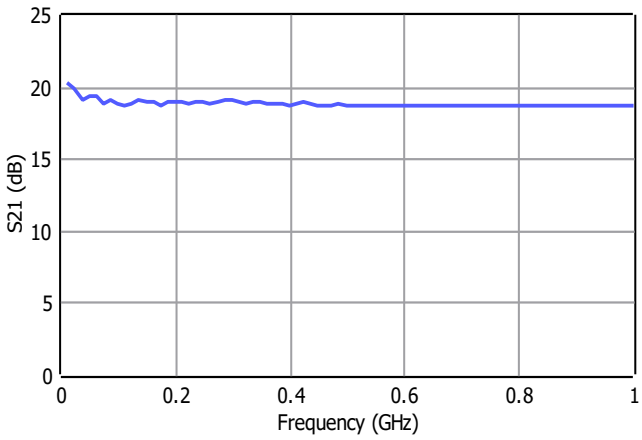
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T = 25 C, LNA State.

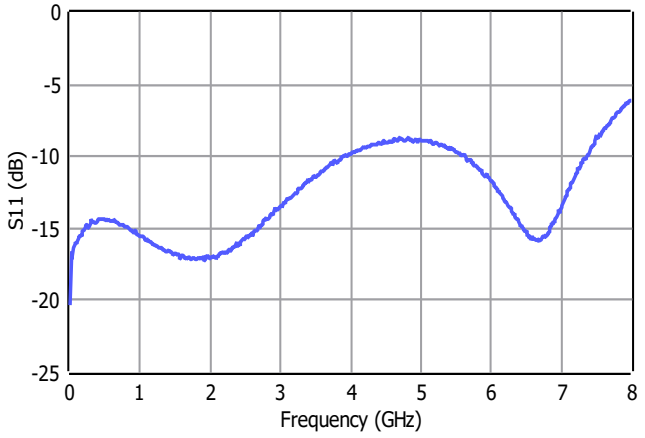
S21 Wideband



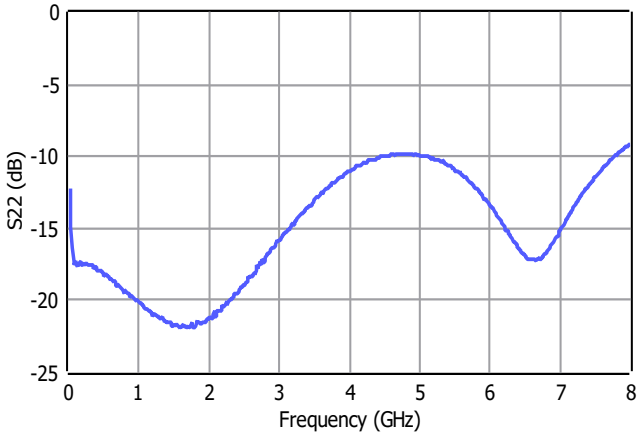
S21 Low Frequency



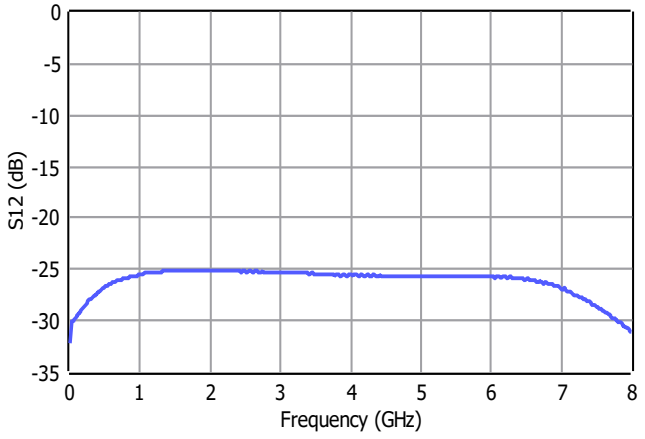
S11



S22



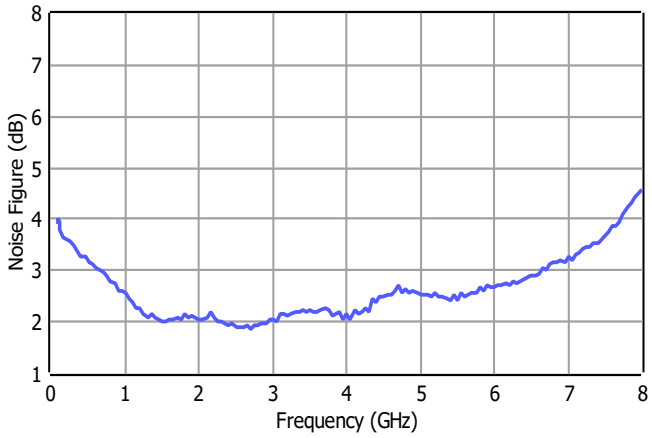
S12



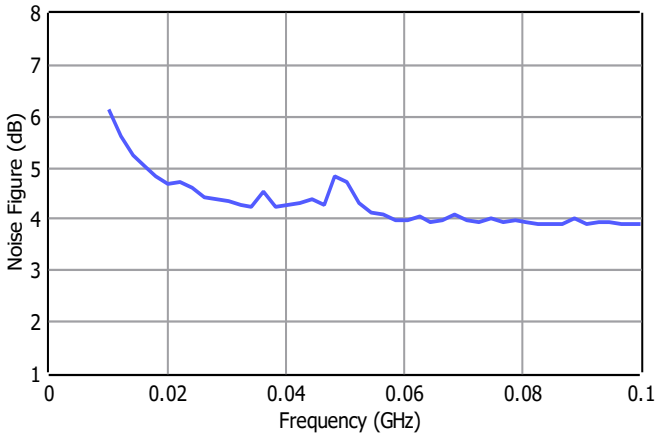
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T = 25 C, LNA State.

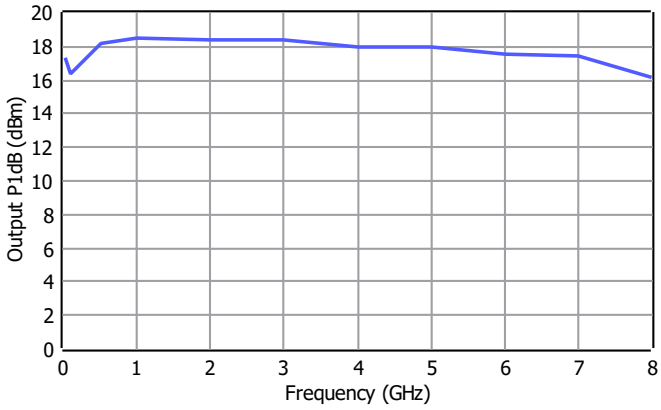
Noise Figure Wideband



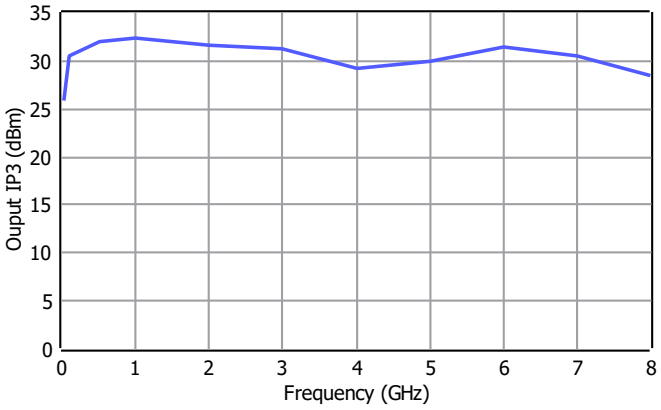
Noise Figure Low Frequency



Output P1dB



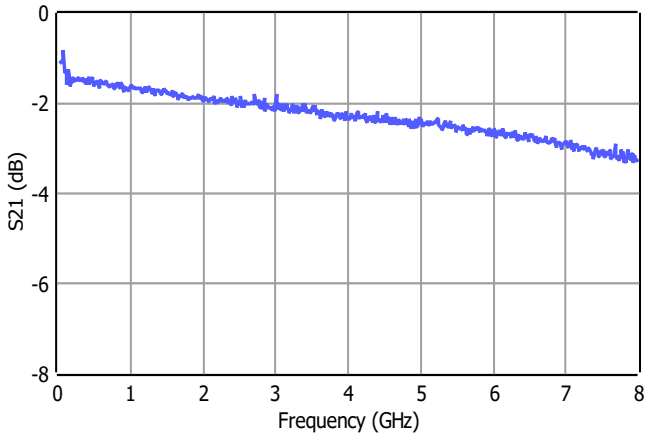
Output IP3



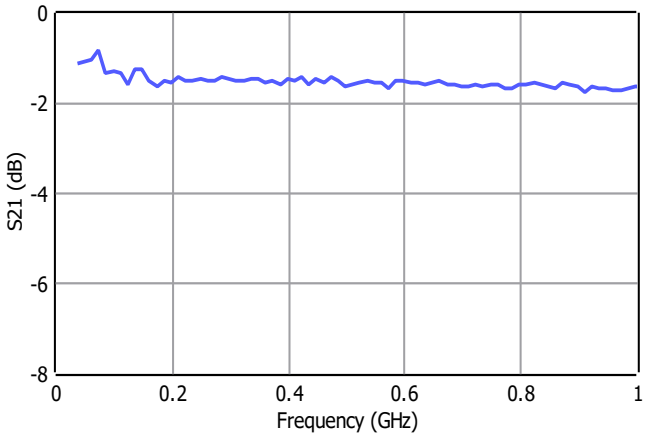
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 5 V, T = 25 C, Bypass State.

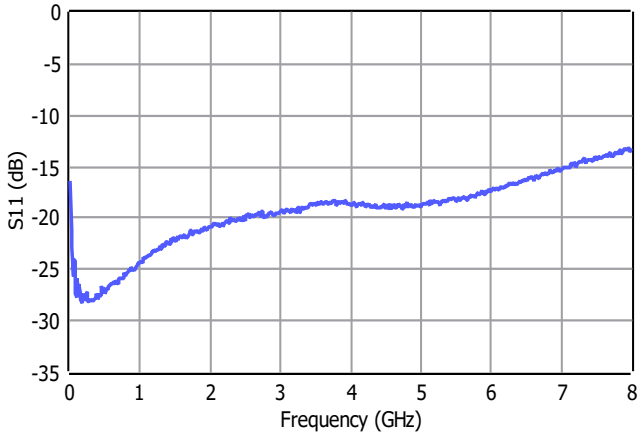
S21 Wideband



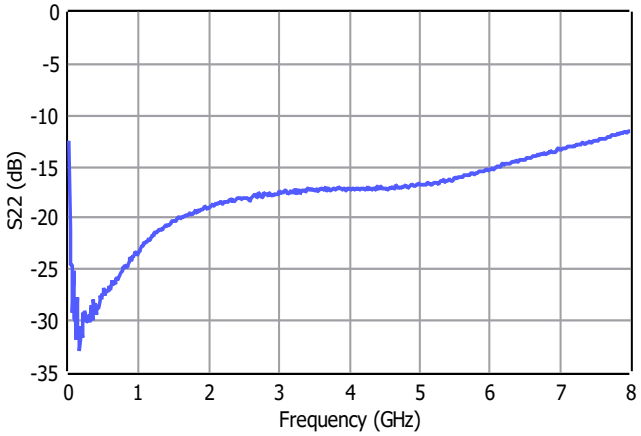
S21 Low Frequency



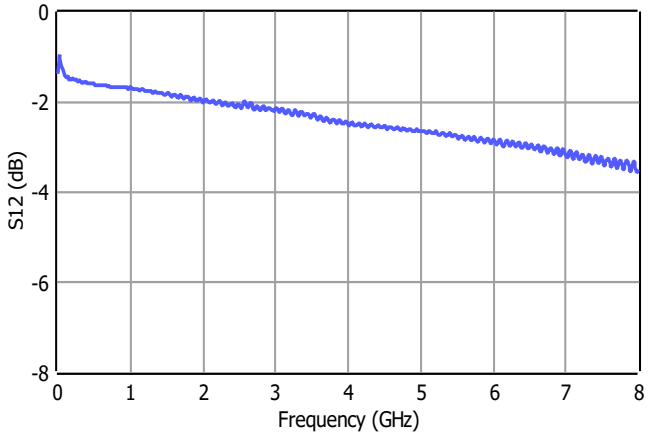
S11



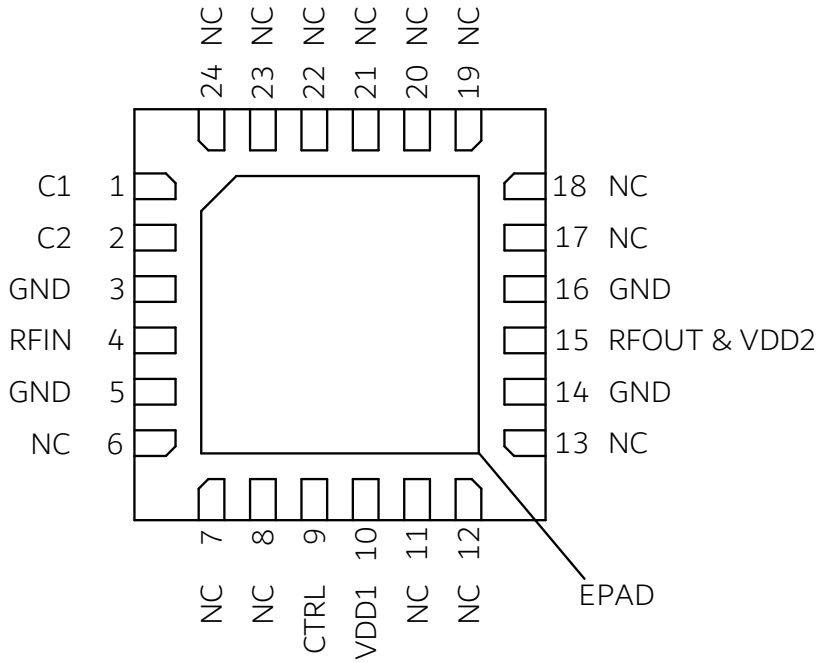
S22



S12



Pin Description



Top View

Pin Number	Pin Name	Description
4	RFIN	RF input pin. Wideband external DC block capacitor is required.
15	RFOUT & VDD2	RF output and Vdd supply pin. Wideband external DC block capacitor and choke inductor are required.
10	VDD1	Vdd bias.
9	CTRL	Control voltage pin.
1	C1	External capacitor connection pin.
2	C2	External capacitor connection pin.
6-8,11-13, 17-24	NC	These pins are not internally connected. Can be grounded on the PCB.
3, 5, 14,16	GND	Ground.
25	EPAD	Exposed Pad on the bottom of the package should be connected to ground with multiple number of vias to reduce the inductance to the GND.

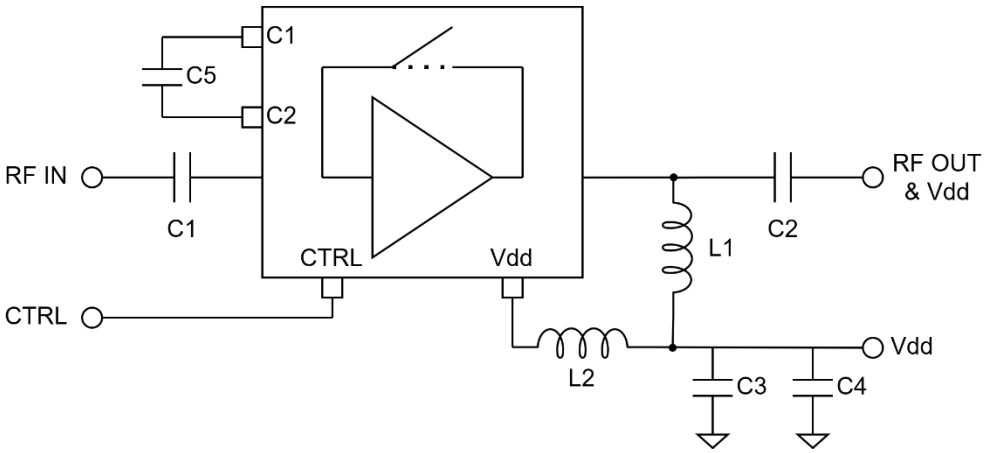
Control Interface

CTRL	State
HIGH	LNA
LOW	Bypass

Applications Information

Signal entering from RF IN goes to RF OUT with an amplification or internal bypass path depending on the state set by the user.

Typical application schematic to operate the bypass amplifier is given below.



C1 and C2 are DC block capacitors. It is recommended to use wideband low loss DC block capacitors to achieve the best performance. Using low profile capacitors is also possible, which will result in additional loss.

L1 and L2 are used as RF choke inductors. It is recommended to use wideband RF chokes to achieve wideband performance.

Choosing higher values for C1, C2, L1 and L2 will allow amplifier to operate at lower frequencies, compared to the plots that is given in this datasheet. By increasing values of these components, low frequency operation can be extended below 10 MHz, at the expense of flat wideband, and high frequency response.

C3 and C4 are used to filter out the ripples and unwanted signals coming from the Vdd supply. Using additional capacitors in parallel to C3 and C4 will improve this filtering. If this filtering is of no concern, then amplifier can be operated without C3 and C4.

Noise figure data is generated with connectorized evaluation PCB measurements. Then the input loss of the PCB is de-embedded from the noise figure measurement data across frequency, to generate the noise figure data shown in this document.

The NC pins of the Amplifier are connected to the GND on the PCB used to generate the plots shown in this document.

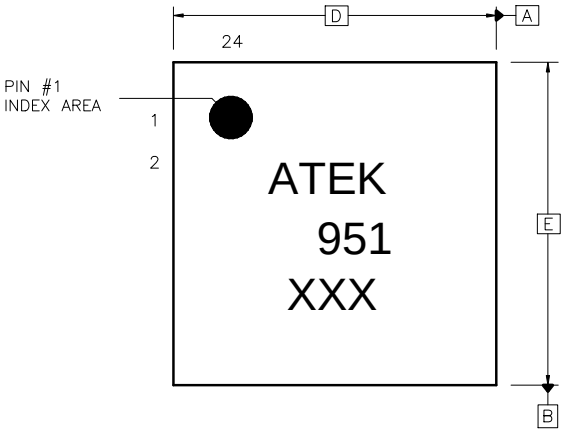
Vdd values shown on the datasheet correspond the Vdd pins shown on the application schematic, not the pins of the amplifier. Vdd value can be increased to get higher P1dB performance.

Absolute Maximum Ratings

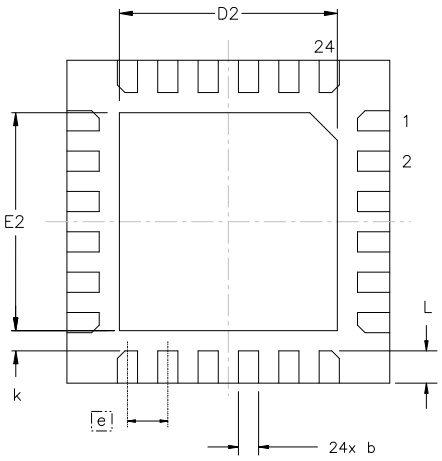
Parameter	Value/Range
Supply Voltage (Vdd)	TBD
Control Voltage (CTRL)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

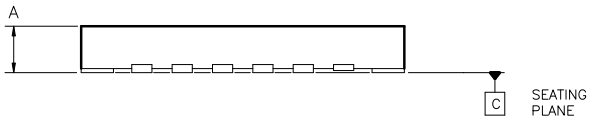
Mechanical and Marking Information



Top View



Bottom View



Side View

NOTES:
1) ALL DIMENSIONS IN MM

SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A, V	0.80	1.00	E2	2.60	2.80
b	0.18	0.30	e	0.50 BSC	
D	4.00 BSC		k	0.20	–
D2	2.60	2.80	L	0.35	0.45
E	4.00 BSC				

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	24.02.2021	Initial Release	
1.1	14.07.2021	Plot Add	4/9
1.2	01.07.2022	Format and Content Fixed	
1.3	10.08.2022	Pin Description Revised	
1.4	16.09.2022	Electrical Specifications Revised	
1.5	25.05.2023	Electrical Specifications, Pin Description and Mechanical and Marking Information Revised	
1.6	14.05.2024	Electrical Specifications Revised	